INCLUDING DEFENSE TECH WIRE

Military EMBEDDED SYSTEMS

June 2012
Volume 8 | Number 4
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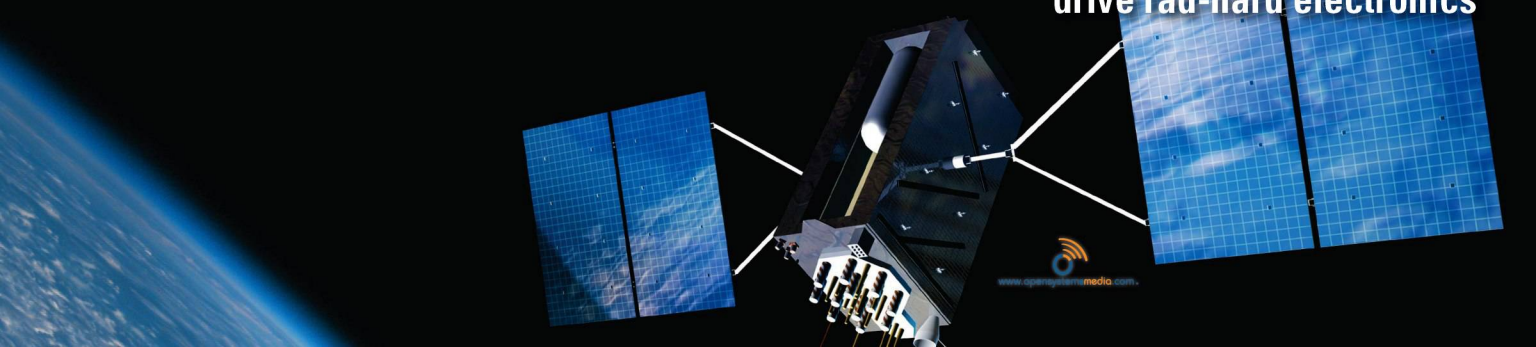
ITAR compliance is mission-critical task for defense suppliers

Floating-point coprocessors enable FPGAs to replace DSPs, by Jeff Milrod, BittWare

See also:

Payload requirements drive rad-hard electronics



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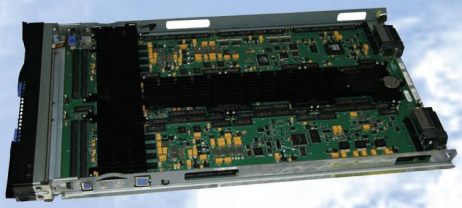

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ON THE COVER:

Top photo: An Alaska Air National Guard HH-60G Pave Hawk helicopter crew practices flight formation maneuvers over Joint Base Elmendorf-Richardson, Alaska, March 14, 2012. U.S. Air Force photo by Master Sgt. Sean Mitchell.

Bottom photo: The GPS III satellite from Lockheed Martin makes use of radiation-hardened electronics for its payload and control systems. Photo courtesy of Northrop Grumman, whose Astro Aerospace business unit supplies self-deploying, monopole JIB antennae for the satellite.

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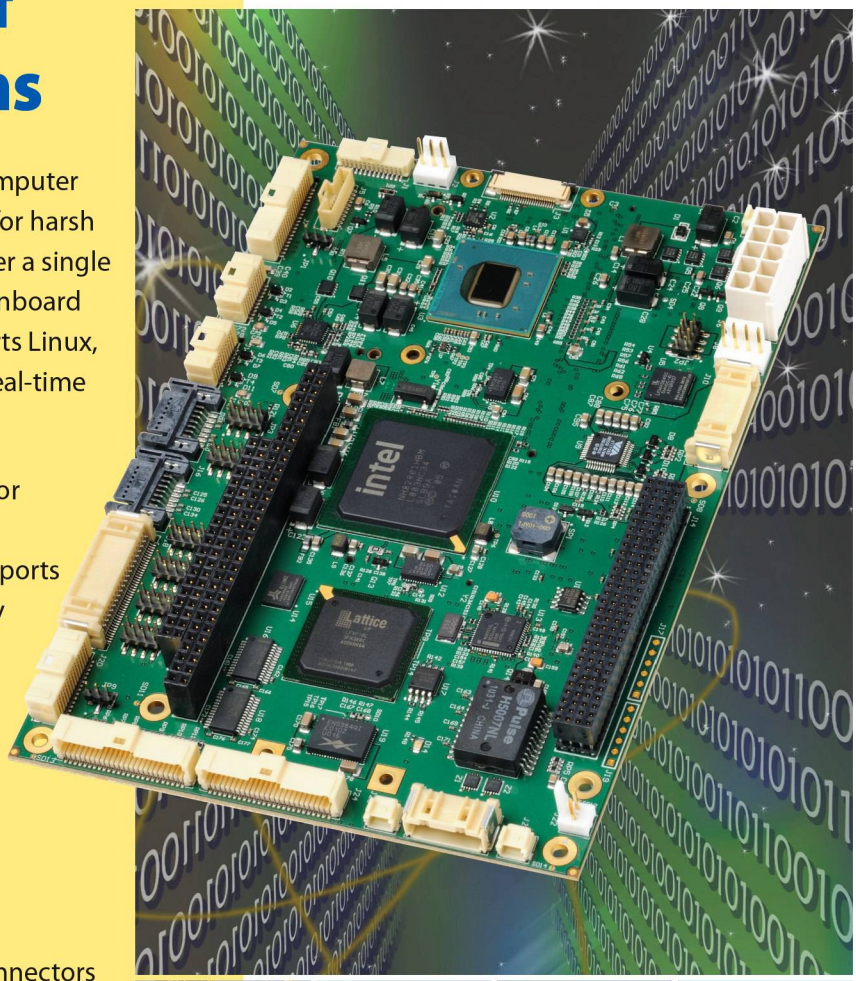

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ITAR fines can cripple your business

By John McHale, Editorial Director

Many in the defense industry community are familiar with export regulations such as the International Traffic in Arms Regulations or ITAR and the nasty punishments the government will level against those who neglect to comply or fail to obtain the proper licenses. However, newcomers to this market might not know how severe the penalties for export compliance missteps can be.

Recent punishments have ranged from $20,000 to as much as $78 million. Yes, you read that correctly – $78 million. Not only that: If you are being investigated for a potential ITAR violation, the State Department can shut down your operation, preventing you from shipping or receiving products. While the Obama administration is exploring various export reform initiatives, the increased enforcement of these regulations is unlikely to abate any time soon. There is also no shortage of enforcement officers, and they like to keep busy.

Detailed listings of fines and ITAR violations can be found at this State Department website: www.pmddtc.state.gov/compliance/consent_agreements.html. I've summarized a couple of the larger one's fines/punishments here, such as the hefty $78 million civil penalty that was leveled against BAE Systems in 2011.

The Department of State charged BAE Systems plc – not the North America subsidiary, BAE Systems Inc., – with violations of the Arms Export Control Act (AECA) and ITAR – 2,591 violations in total and as far back as 1995. Some of the violations included failure to obtain U.S. State Department approval "to engage in brokering activities of the U.S. systems or subsystems" on platforms including the Hawk Trainer aircraft, the EF-2000 Eurofighter Typhoon, and the Saab Gripen aircraft prior to the sale of those aircraft to multiple foreign nations, according to the Department of State proposed charging letter to BAE Systems from May 2011. In other words, any time electronics on the U.S. Munitions List (USML) are added or modified, proper approval must be obtained before companies can export the systems.

Companies are not the only perpetrators that get nailed by the government for export violations. Individuals charged under AECA or ITAR can get extensive jail time because this is a crime. The victim of the crime is the soldier, marine, sailor, pilot, or airman whose life might be endangered by American technology falling into the wrong hands.

> *"While the Obama administration is exploring various export reform initiatives, the increased enforcement of these regulations is unlikely to abate any time soon. There is also no shortage of enforcement officers, and they like to keep busy."*

Examples where jail time was handed out can be found on the State Department's website in a Justice Department pdf document that covers major U.S. export enforcement and embargo criminal cases dating back to 2007 (www.pmddtc.state.gov/compliance/documentsOngoingExportCaseFactSheet.pdf). Check it out, it reads like a police blotter.

One of those cases, dated December 3, 2010, details the illegal sale of radiation-hardened (rad-hard) semiconductor components to China. Lian Yang of Woodinville, WA, was arrested and charged with conspiracy to violate the AECA by attempting to purchase and export from the U.S. to China 300 rad-hard, programmable semiconductor devices, which are classified as defense articles under the U.S. Munitions List. According to the Justice Department document, Yang and his co-conspirators were busted in an undercover operation when they wire-transferred $60,000 to undercover agents for partial payment on some of the devices. Agents from ICE, CBP, and the FBI conducted the investigation. (To read about law-abiding rad-hard electronics suppliers, see our Mil Tech Trends section, beginning on page 20.)

U.S. export controls, while useful in protecting American technology from rogue nations, have also been a detriment for defense technology suppliers wanting to be competitive on a global scale – especially in the commercial satellite industry. The DoD and industry are currently lobbying Congress to have satellites and related devices not containing technology vital to the U.S. military taken off the U.S. Munitions List and designated as dual-use items on the Commerce Control List (CCL). This would be a huge boost to U.S. satellite component designers who want to grow their business but feel handcuffed by ITAR regulations. The effort is called the *1248 Report* and is covered in our Special Report on ITAR compliance, beginning on page 16. Also in that article, export attorney Kay Georgi of Arent Fox, LLP, talks about the latest enforcement trends and gives tips on how to set up a compliance program.

The best tip I heard was from an attendee at an ITAR panel discussion a few years ago: Assume everything is ITAR-controlled and cover your back because you don't want to get that letter from the State Department.

John McHale
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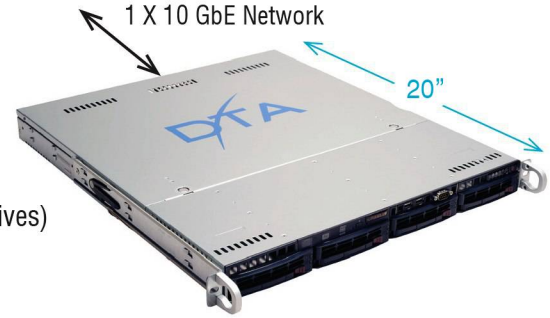

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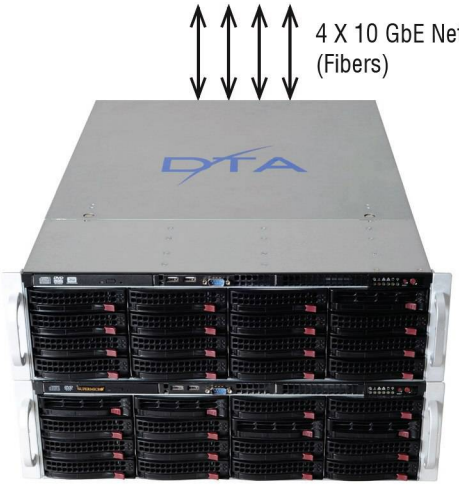

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Honey, I shrunk the data center

By Charlotte Adams

A GE Intelligent Platforms perspective on embedded military electronics trends

Why are defense chip and board developers turning to the InfiniBand switched fabric interconnect technology? Though blazing fast, InfiniBand is neither new nor widely used in Department of Defense (DoD) weapons and platforms. But a new InfiniBand-on-VPX paradigm is coming to high-performance embedded computing to meet the needs of Intelligence, Surveillance, and Reconnaissance (ISR) and similar demanding applications.

Advantage of InfiniBand

InfiniBand provides high-speed, point-to-point bidirectional serial links between fabric nodes. The reason it is becoming attractive in high-performance embedded computing is because of InfiniBand's market penetration into platforms such as the top 500 high-performance computing clusters, large data centers, market trading floors, and cloud computing environments.

In fact, according to a press release from the InfiniBand Trade Association late last year, 42 percent of the world's most powerful computers listed at www.top500.org use InfiniBand. The number of cores connected via InfiniBand has increased 24 percent year on year. These platforms, some of which comprise tens of thousands of Intel and NVIDIA processors, have driven the development of extremely robust software support at the operating system, middleware, and driver levels.

VPX and InfiniBand

Developers are also combining InfiniBand with VPX, a point-to-point serial backplane interconnect that is the migration path for VME. VPX shares form factors with VME but has many advantages over the workhorse parallel bus used in many embedded military and aerospace applications. VPX offers at least an order of magnitude increase in data rates over VME. Although each VPX link sends only a few bits at a time, the data rate is so high that card-to-card transfers can reach more than 100 GBps. Additionally, multiple receivers and transmitters can communicate at the same time.

VPX is a multiplane technology that allows data crunching, expansion, control, management, and utility tasks to be executed separately and simultaneously on their respective planes, improving overall speed and efficiency. VPX is also agnostic to physical protocols, making it highly flexible. For example, on the data plane, designers can implement InfiniBand, 10 GbE, PCI Express, or Serial RapidIO. VPX is flexible, offering a wide range of possible architectures. Indeed, so wide is the possible range of architectures that VITA, the VME trade association, has formed an umbrella OpenVPX (VITA 65) working group to develop a set of standard backplane topologies to facilitate the development of modular open-system architectures.

Figure 1 | The SBC625 from GE Intelligent Platforms, a 6U VPX board using Intel's 2.3 GHz Core i7-3615QE processor

Ripe ecosystem

The InfiniBand software ecosystem, there for the taking, begs to be used by the high-performance applications typical of many military and aerospace projects. It correlates directly with the DoD's need, now more than ever, to exploit commercial development, minimize costs, and protect existing investments.

Driving adoption are data-hungry but space-constrained applications in areas such as ISR, signals intelligence, electronic warfare, and communications. For example, relatively small packages on drones are expected to crunch floods of data from front-end sensors and provide actionable information in real time. To do that, they need not only higher data throughput but higher interboard communications, for which InfiniBand-on-VPX offers an attractive solution. Drones are just one potential platform. Others include aircraft, submarine, and satellite sensors where high speed and bandwidth are needed but real estate is scarce.

Ready for prime time

A number of embedded computing developers are working on InfiniBand/VPX products in combination with Intel's latest Core i7 products. A case in point is the SBC625 from GE Intelligent Platforms, a 6U VPX board using Intel's 2.3 GHz Core i7-3615QE processor (Figure 1).

InfiniBand is optimized for very high-throughput, low-latency data traffic. It fits well with multicore processors and supports Remote Direct Memory Access (RDMA), General-Purpose Computing on Graphics Processing Units (GPGPU), and Open Fabrics Enterprise Distribution (OFED) open-source software, among other advantages.

According to the InfiniBand Trade Association, OFED adoption and deployment are increasing, largely because it helps RDMA-based networks provide computing efficiencies as high as 96 percent and latencies as low as 1 microsecond, as well as reducing data center power consumption by up to 50 percent.

The bottom line is that InfiniBand with VPX brings together the software created for high-performance supercomputers in a rugged, backward-compatible format, creating a powerful synergy for defense and aerospace applications.

Contact Charlotte at cburtonadams@yahoo.com.

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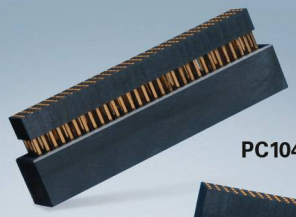

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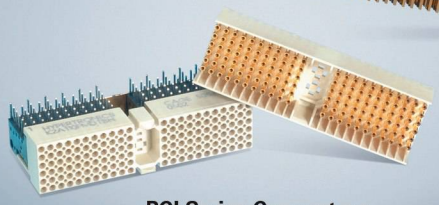

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Managing ITAR compliance in COTS systems design

By Curtis Reichenfeld
An industry perspective from Curtiss-Wright Controls Defense Solutions

As foreign sales continue to be a key driver for many U.S. vendors, it is critical to ensure due diligence of the International Traffic in Arms Regulations (ITAR) to avoid profile violations and penalties.

ITAR is the set of export control regulations implemented and enforced by the U.S. State Department's Directorate of Defense Trade Controls (DDTC) that controls the export of defense articles, defense services, and technical data as designated on the U.S. Munitions List (USML). Under ITAR, defense articles are items specifically designed, developed, or manufactured for military or defense purposes. These include commercial items that have been modified for a military purpose. Certain technical assistance services related to defense or military purposes are known as *defense services*. Defense services can include activities such as repairs, training, engineering, testing, and product assembly. Technical data might include documents, drawings, schematics, design information, data sheets, and so on that reveal technical data directly relating to items on the USML.

The U.S. Department of Commerce's Bureau of Industry and Security (BIS) implements and enforces the Export Administration Regulations (EAR) that regulate the export and re-export of most commercial items. This includes "dual-use" items with both commercial and military or proliferation applications. It also includes purely commercial items without obvious military use. License requirements depend upon an item's technical characteristics, the destination, the end user, and the end use. The exporter must make the determination if an export requires a license. While other regulations can be relevant, the EAR and ITAR are the most frequently applied and regularly encountered sources of control for high-technology industries.

Typically, manufacturers can self-classify their items by reviewing the ITAR and EAR. If the manufacturer is uncertain of an item's classification, they can get assistance by submitting a Commodity Jurisdiction (CJ) request to DDTC. A CJ is a process that outlines how export control jurisdiction is determined, which is the first step in analyzing an item's overall export control classification. DDTC, in cooperation with BIS, can classify the product as "dual use," which includes civil and some military applications, or "commercial," and can further provide the full classification number. Neither dual-use items nor commercial items fall under the ITAR.

Product development process

ITAR issues should be considered during the product development process, before design and manufacture, to ensure equipment is ITAR free. At Curtiss-Wright Controls Defense Solutions, during the first part of an IRAD approval process, we focus on a product's high-level requirements. Product descriptions should be written with the ITAR in mind and then reviewed by export compliance experts. Involve the export control officer early to make a determination if the product can be classified as ITAR free.

During product design, use commercially available components and software algorithms to reduce the risk that the product can fall under the ITAR. If commercial parts are not available or the application requires military-grade chips, companies need to follow the regulations and can apply for a CJ.

Common mistakes

Some of the common compliance errors COTS vendors need to avoid include:

- **Failure to hire a compliance expert** – Hiring a dedicated export control officer experienced in working with the Department of State and ITAR is essential for ensuring compliance.
- **Failure to maintain detailed records** – Start with an export compliance plan and keep detailed records documenting the plan implementation, including any self-classifying of products. CJ applications also require providing records of product background and sales information. Documentation associated with all exports of items or defense articles, defense services, and technical data must be retained by the exporter.
- **Reclassification of products** – Legacy products might need to be reclassified as items fall off the ITAR USML or EAR Commerce Control List. Export control officers should review products regularly and determine if classification or application for a CJ is needed.
- **Too focused on sales** – Many companies, while focusing on sales and generating new business, lose sight of ITAR compliance. They need to dedicate the appropriate time for reviewing products and obtaining licenses in advance of a sale.
- **Poor training** – Proper training and awareness ensure that employees understand ITAR compliance and know to ask the proper questions when they experience issues with products that could be controlled items. Companies need to document an export compliance plan that is tied to company procedures and then invest in training.

Ignorance of the ITAR is not a valid defense against violations of the regulations. When in doubt, apply for a CJ determination to ensure the jurisdiction of products and seek the assistance of an experienced export compliance person to determine export license requirements. With proper due diligence, new markets for U.S. companies are available worldwide.

This column is a synopsis of a high-level white paper written by Curtis. For more information, e-mail Curtis at Curtis.Reichenfeld@curtisswright.com.

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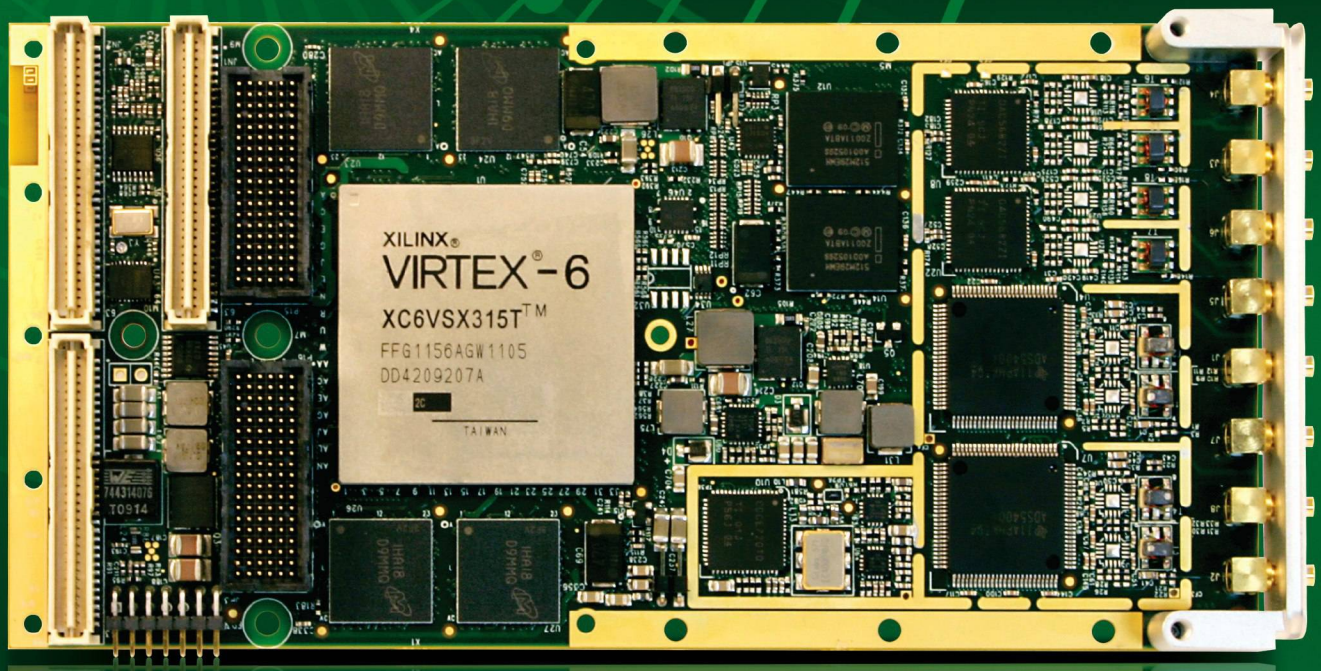

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By Sharon Hess, Managing Editor

NEWS | TRENDS | DoD SPENDS

U.S. Navy Trident II production occurs the conventional way

While fictional movie character Tony Stark of "Iron Man" fame made it look easy to make a missile-shooting armored exoskeleton while in captivity, in reality missile production is a complicated process requiring many resources. And apparently – per a $236 million U.S. Navy contract – semi-namesake real-life company Charles Stark Draper Laboratories, Inc. is slated to render alteration materials for the Trident II (D5) missile guidance systems' production (Figure 1). Work will ensue in El Segundo, CA; Clearwater, FL; Cambridge, MA; Pittsfield, MA; and Tarrytown, NY, and is anticipated for fulfillment by September 2016.

Figure 1 | A $236 million U.S. Navy/Charles Stark Draper Laboratories, Inc. contract calls for alteration materials for Trident II (D5) guidance systems' production. U.S. Navy photo by Seaman Benjamin Crossley

Laser JDAM sensors to be onboard more military aircraft

The Boeing Company's Laser Joint Direct Attack Munition (Laser JDAM) sensors will soon find themselves on more U.S. military aircraft, per a $12.5 million U.S. Naval Air Systems Command (NAVAIR)/Boeing contract. JDAM is a guidance kit that is "low cost" and transforms "existing unguided freefall bombs into near precision-guided weapons," according to the Boeing website. JDAM enables moving target, relocatable target, and maritime threat prosecution. The laser sensor added to traditional JDAM is a relatively straightforward option to implement for pilots who have been using conventional JDAM, Boeing reports.

Northrop Grumman to upgrade USAF production pods

The U.S. Air Force's pods are due for some sprucing up by Northrop Grumman Technical Services, thanks to a recent $52 million pod upgrade program contract. The contract calls for "nonrecurring engineering services for [the] engineering manufacturing development phase," prototype upgraded pods (4),and modified support equipment sets (2); "low rate initial production support equipment will be a basic contract option manufacturing development phase," according to the DoD website. Northrop Grumman will also provide anywhere from 1 to 12 equipment kits for production pod support. Work occurs in Warner Robins, Georgia, and completion is anticipated in April 2017. The contracting activity is Robins Air Force Base in Georgia.

Test sets ensure USAF planes are in tip-top shape

All USAF aircraft must have their flight control systems tested; thus, a recent $8 million contract between the USAF and Custom Manufacturing & Engineering, Inc. has the latter providing the former with flight control systems test sets that will be utilized by every Air Force program (Figure 2). "The flight control system test set tests, calibrates, and troubleshoots weapons systems equipment with reduced vertical separation minimum," the DoD website says. The test sets additionally generate static and regulated pilot pressures for use in analyzing pneumatic instruments, auxiliary equipment, and air data systems of the aircraft. Work is slated for completion in Pinellas Park, FL, by April 2018. The contracting activity is Robins Air Force Base in Georgia.

Figure 2 | A recent $8 million USAF contract has Custom Manufacturing & Engineering, Inc. providing flight control systems test sets to be utilized by every USAF program. Pictured: The HH-60G Pave Hawk, U.S. Air Force photo by Master Sgt. Sean Mitchell

JSF hardware and software changes coming

Though they might appear identical at first glance, the U.S. Navy granted Lockheed Martin Corp. two different-yet-similar contract modifications on the same day: 1) A $68 million modification for changes to baseline software and hardware configurations for the F-35 Lightning II Joint Strike Fighter/JSF (Figure 3); the government-requested alterations include short take-off vertical landing (USMC) and conventional landing and take-off (USAF) as a modification to an LRIP II contract. Funding comes from the U.S. Navy and USAF. 2) A nearly $46 million F-35 Lightning II Joint Strike Fighter contract modification to an LRIP III contract also calls for baseline software and hardware changes, as required by the United Kingdom and the USMC for short take-off vertical landing. Funds are provided by the U.S. Navy and the U.K.

Figure 3 | Two recent contract modifications have Lockheed Martin making baseline software and hardware configuration changes to the JSF under LRIP II and III contracts. U.S. Navy photo of F-35C Lightning II JSF test aircraft courtesy of Lockheed Martin

ALQ-99 tactical jamming system's successor gets more mature

A recent $20.5 million Naval Air Systems Command/BAE Systems, Information and Electronic Systems Integration, Inc. contract modification stipulates that BAE renders next-generation jammer-supportive technology maturation. The next-generation jammer is, logically, slated as the successor to the aging tactical jamming system dubbed "ALQ-99." Efforts under the contract comprise research to enable future airborne electronic attack abilities proffered by an airborne stand-off/mod-escort platform that is tactical-sized. Thus, BAE will give Naval Air Systems Command a Concept Demonstrator (CD) design in addition to the needed mature technology elements that will support design of the Concept Demonstrator. Work takes place in Baltimore, MD; Lansdale, PA; Cincinnati, OH; Melbourne, FL; and Nashua, NH, and is anticipated to be done by April 2013.

For consideration in Defense Tech Wire, submit your press releases at http://submit.opensystemsmedia.com. Submission does not guarantee inclusion.

Figure 4 | The U.S. Army and General Dynamics Land Systems signed a contract and a modification providing vehicles and technical services for Abrams tanks. M1A2 SEP V2 tanks photo by Mollie Miller, 1st Inf. Div. Public Affairs, U.S. Army

M1A2 Abrams spotlighted in contract and modification

The U.S. Army and General Dynamics Land Systems put pen to paper twice on one day, to benefit the venerable Abrams tank. First, a $31 million contract calls for "the procurement of 46 Abrams M1A2 system enhancement package V2 vehicles [Figure 4]," with work slated for Anniston, AL; Scranton, PA; Lima, OH; and Tallahassee, FL, according to the DoD website. Work is anticipated for completion in November 2014. Second, a separate contract modification has General Dynamics Land Systems providing technical services for the Abrams Tank Program. Work is due for completion this December.

ASU to develop a health-monitoring system for warfighters

And the (contract) award goes to … Arizona State University (ASU). Specifically, the Defense Threat Reduction Agency recently awarded ASU a Research, Development, Test, and Evaluation (RDT&E) contract comprising a 12-month performance base period with a $9 million value in addition to a 36-month $21,500 option. ASU's mission is to design a fieldable, chip-based, warfighter health-monitoring system prototype that can identify health changes of the warfighter (Figure 5). The goal is early infection detection. The contract's work will occur at Tempe, AZ.

Figure 5 | ASU will design a fieldable, chip-based, warfighter health-monitoring system prototype per a recent contract from the Defense Threat Reduction Agency. U.S. Army photo by Spc. Cassandra Monroe

ITAR compliance is a mission-critical task for defense suppliers

By John McHale

Even though the U.S. government is entertaining various forms of export compliance control, defense suppliers must continue to be vigilant when dealing with the ITAR and other export regulations or face multimillion-dollar fines for failing to comply. Meanwhile, potential reforms to spacecraft export rules potentially could be a big win for rad-hard electronics vendors.

Suppliers of electronics for military platforms – such as these National Guard HH-60G Pave Hawk helicopters flying over Alaska – must have the appropriate export licenses or they will face business-crippling fines. U.S. Air Force photo by Master Sgt. Sean Mitchell.

Producing embedded electronics for military applications requires that defense suppliers meet stringent environmental and performance standards on the design side so that the technology does not fail in the field. Compliance with U.S. export control regulations such as the International Traffic in Arms Regulations (ITAR) also is essential because failure to comply could lead to multimillion-dollar fines that could shut down their business completely.

ITAR and export compliance regulations have been around for decades, but the past decade has seen record fines and increased enforcement of export controls by the U.S. government. Contributing to this are companies that have little experience with export compliance looking to break into the steady military market to stem losses in more volatile commercial markets.

Also many experienced companies think they know the difference between a component that needs an ITAR license and one that does not or is classified as dual-use. "Dual-use has been used as a shorthand for describing items subject to the Export Administration Regulations (EAR)," says Kay Georgi, an export compliance attorney and Partner at Arent Fox LLP in Washington, D.C. Commerce in its proposed rule published July 15, 2011 "gave this definition: 'A dual-use item has commercial applications and also has military applications or proliferation concerns.'"

Enhanced export compliance enforcement makes it tough for U.S. companies to do business abroad in the global economy and also frustrates foreign companies looking to sell to the U.S. or to resell systems that have components of U.S. origin. The Obama Administration is working on overall compliance reform across multiple agencies, but these reforms still have to be approved by Congress.

Export compliance reform

"The Administration continues to make great progress towards developing a single control list," Georgi says. "To date, they have published proposed rules on: military aircraft; gas turbine engines; military vehicles; military vessels of war; submersibles; spacecraft through Report DoD 1248 from Departments of State and Commerce; and explosives and energetic materials, propellants, incendiary agents, and their constituents."

"These proposed rules would move many U.S. Munitions List (USML) controlled items to the Commerce Control List under special 600 Series Export Control Classification Numbers (ECCNs) that will continue to require licenses to most destinations, although some items may benefit from license exception Strategic Trade Authority (STA) for end use by the governments of some countries," Georgi says. "The proposed rules are still to be sent to Congress,

and of course, they still do not combine the Commerce Control List (CCL) and the USML into a single list. Indeed, some would say the addition of the 600 Series to the CCL effectively creates two lists within the CCL, but still these are substantial steps towards export control reform. A U.S. government official recently went on the record stating that the Administration hopes to send the necessary reports for a number of the USML categories to Congress as soon as August 2012. It remains to be seen if this ambitious schedule can be kept, as a number of proposed regulations need to be sent out for notice and comment first, but it indicates that the Administration continues to press forward briskly even in an election year."

Space export control policy reform: Section 1248 Report

The aforementioned Section 1248 Report is an effort by State and DoD officials working with the space industry to revamp space export control policy. Congress requested the report in Section 1248 of the National Defense Authorization Act for Fiscal Year 2010 (Public Law 111-84), according to a DoD release.

"In the DoD 1248 report, the Departments of State and Defense concluded that certain satellites and parts and components did not warrant continued control on the USML," Georgi says. "More specifically: 'Communications satellites (COMSATs) that do not contain classified components; remote sensing satellites with performance parameters below certain thresholds; and systems, subsystems, parts, and components associated with these satellites and with performance parameters below thresholds specified for items remaining on the USML.'"

"The current environment, which has rad-hard ICs covered under the ITAR, is destroying the satellite industrial base and is hurting the second- and third-tier suppliers," says Chuck Tabbert, Vice President at Ultra Communications in Vista, CA, and a member of the President's Export Council Subcommittee on Export Administration (PECSEA). "If the recommendations of the 1248 Report are implemented, it could mean that radiation-hardened ICs will move to the Department of Commerce with a special export commodity control number, which by utilizing the new STA exception could allow us to ship to 36 nations without having a license required."

The Departments of State and Defense concluded that certain other satellites and parts and components did warrant continued USML control, such as satellites performing purely military or intelligence missions; remote sensing satellites with high-performance parameters; systems, subsystems, parts, and components unique to the aforementioned satellite types and not common to dual-use satellites; and services supporting foreign launch operations for USML- and CCL-designated satellites, Georgi says. To view the entire report, visit www.defense.gov/home/features/2011/0111_nsss/docs/1248_Report_Space_Export_Control.pdf.

Tabbert says the reform will enable "friendly countries to sell to other friendly countries without getting U.S. permission first. They would be able to sell to European satellite manufacturers of COMSATs like Thales and EADS Astrium, which support Inmarsat, Eutelsat, etc. Another implication is that it will strengthen relationships with foreign partners. The government is still concerned about working with China in the space area, and the 1248 did not recommend a change to that practice."

The report essentially says that if even one U.S.-origin connector is on a European-made satellite exported to China, it would require a license and be denied, Georgi says. "A license would still be required under the ITAR for a U.S. person to provide any assistance to a foreign person for a spacecraft to be launched from outside the U.S., even if that spacecraft may be exported under License Exception STA. Launch services and launch failure analysis for the CCL satellites and parts also remain subject to the ITAR," Georgi continues. "Since those selling spacecraft would normally need to provide some support for their launch, this effectively means that an ITAR license [presumably a Technical Assistance Agreement (TAA)] would still be needed to sell a U.S. CCL satellite to a non-U.S. or U.S. customer for launch outside the U.S."

Enforcement trends

"We are beginning to see the fruit of the export enforcement portion of the export control reform initiative in the creation of three cross-agency enforcement units," Georgi says. "How these coordination units will change the enforcement landscape remains to be seen, but I anticipate they will ensure a greater degree of coordination of efforts between the many agencies enforcing the export control laws."

One key coordination unit is the Export Enforcement Coordination Center (E2C2), which is housed at Immigration & Customs Enforcement and is a clearinghouse for coordinating enforcement activities among the Departments of Homeland Security, Commerce, Energy, Treasury, State, Justice, and the Director of National Intelligence, she says. A

second unit is the Information Triage Unit (ITU) in Bureau of Industry and Security that operates as a forum for assembling and disseminating information and intelligence gathered by agencies across the government so that individual export licensing agencies will have a consistent data set, Georgi continues. The third unit is the Office of the National Counterintelligence Executive (ONCIX), which coordinates export control issues involving the intelligence community.

"On the criminal side, I believe we are seeing greater crossover between export control cases and other cases, specifically in the areas of [the] Foreign Corrupt Practices Act (U.S. v. BAE Systems in 2010 and U.S. v. Shu Quan-Sheng in 2009) for ITAR Part 130 violations, the False Claims Act, and perhaps more than any other, the Economic Espionage Act (EEA)," Georgi continues. "While the EEA/export control prosecutions have largely targeted individuals, these have definitely been on the rise. In some cases, EEA prosecutions involve trade secrets that are not export controlled so there is not a perfect overlap between the two." For more on ITAR penalties, see the Editor's Perspective column on page 8.

A tough area for the government to enforce export violations is in cyberspace. Many small companies do not have the IT infrastructure to prevent access by unauthorized entities or persons, so "sophisticated intrusion attempts are on the increase, and some companies may choose to not report the attempt or actual intrusion, believing they may lose present or future business or create bad press," says Dean Young, Celestica Aerospace Technologies Corp. Security Manager in Austin, TX. Cloud services also risk that controlled data will inadvertently be released to unknown entities or countries without

Export compliance in 15 steps

Export compliance in 15 steps

Kay Georgi, an export compliance attorney and Partner at Arent Fox LLP in Washington, D.C., outlines 15 key steps to ITAR compliance.

1) Get management buy-in for your compliance program – If management does not support the program, it likely will not work.
2) Identify two persons in your organization who will be your export compliance personnel – one is not enough. If you do not have good candidates, you may have to recruit from outside your organization.
3) Make sure your export compliance personnel have thorough export control training – For most companies except the largest, this usually means outside training.
4) Classify all the products, services, software, and technology that your company exports. This might mean classifying all items, even if you do not "export" them in the traditional sense, if you employ foreign nationals or procure offshore. Put in your new product development a gate for classification, and put in your new contract review system a gate for classification.
5) Make sure any controlled products are identified in your ERP system or in another fashion so that your personnel will know that they are controlled.
6) Put in place automatic and other gates in your ERP system and in your sales/customer service departments to make sure that any controlled products are not exported, re-exported, imported (for items on the U.S. Munitions List and U.S. Munitions Import List), or transferred without any required license.
7) Put in place a gate in your Returns and Repairs department, to make sure that all returns of defense articles to the U.S. are properly authorized (exemption claimed) and returned pursuant to license or exemption. Also make sure the department recognizes if the item has ended up in the hands of an unlicensed end user.
8) Create a technology control plan to cover controlled technology, and be sure to include IT, human resources, and procurement/purchasing (for offshore procurement) departments in your plan. Put in place measures to identify, correctly label, and protect controlled technology. Create Standard Operating Procedures (SOPs) to do so with the assistance of IT, HR, and procurement departments.
9) Create a license management system, including the export process and filing of Automated Export Records, to ensure compliance with all licenses, license exceptions (EAR), or license exemptions (ITAR).
10) Be sure to screen all customers against the restricted party lists, both at the initial customer input stage and prior to shipment, record, and preserve screens.
11) Train personnel for red flags of prohibited end use and diversion and create a process for resolution of red-flag screening.
12) Create a problem management to deal with issues as they arise, as well as government inquiries and visits.
13) Put all of the aforementioned procedures into a compliance manual and SOPs.
14) Train and test all personnel, or at least most personnel, on the compliance manual and SOPs on a regular basis.
15) Audit regularly, alternating responsible internal auditors (if you have them) with experienced outside auditors. Follow up on audit results. File voluntary disclosures where warranted.

Sidebar 1 | Export compliance attorney Kay Georgi shares 15 tips for ITAR export compliance.

proper authorizations. "We may never know the true extent of data loss in the U.S. involving controlled data and technology."

Avoiding mistakes

Companies and individuals can avoid the attention of export compliance enforcement officials by avoiding some common mistakes. Many of the large prime contractors have strong compliance programs in place, yet individuals at those companies still slip up when it comes to the ITAR. (For steps to setting up a compliance program see Sidebar 1.)

"Typical mistakes these individuals make include not paying enough attention to export compliance, as they are so busy with running the business they don't devote the time necessary to analyze the export control issues associated with a particular transaction," Georgi says. Another is that when an issue arises, they fail to consult legal counsel in-house or outside for assistance. "This is particularly an issue with respect to government inquiries, but it is also true in the case of 'Oops, I think we may have made a mistake.'" A third error is when they assume "they know the export compliance rules and [proceed] without appropriate guidance. If the experts need to check and double-check their advice, the employee who has sat in on an hour of training should not be making the decisions. They need to troubleshoot and take it to the responsible company (empowered) official or legal department."

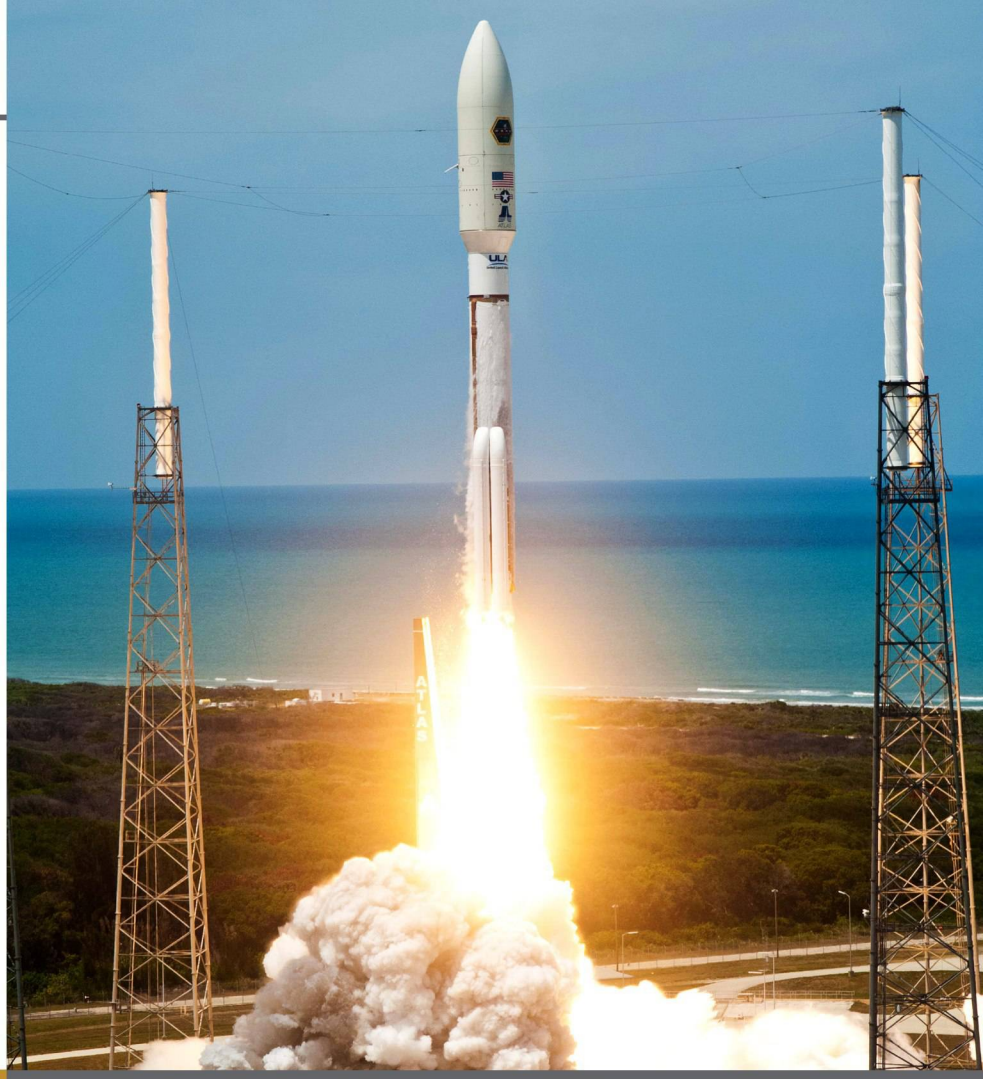
Smaller companies and ones new to the defense market are also prone to easily avoidable ITAR compliance slip-ups. Georgi lists 10 of them:

1) Not realizing their work is subject to ITAR or EAR controls in the first place;
2) Not realizing that even if they do not export, they have to register as manufacturers if they manufacture defense articles in the U.S.;
3) Not knowing which of their projects are ITAR, either because they don't ask the right questions or they don't have the size or knowledge to obtain the necessary information from their (usually much larger) customers with ITAR projects;
4) Not realizing that even if they don't export end product outside the U.S., they can be exporting ITAR-controlled technical data when they procure build-to-spec or build-to-print parts from foreign suppliers or even U.S. suppliers with foreign suppliers;
5) Not realizing that even if they don't export end product outside the U.S., they can be exporting ITAR-controlled technical data when they employ foreign nationals on their ITAR projects;
6) Not devoting enough or the right resources to ITAR and EAR compliance;
7) Too much reliance on a single export compliance official or a fraction of an employee (too-many-hats issue) and not enough training to that person;
8) Not providing all the information needed for a complete and accurate license application;
9) Not following all the provisos/conditions and the regulations in general in exporting pursuant to a license; and
10) Not handling export compliance issues properly, causing them to become larger export compliance issues. **MES**

Military satellite payload performance demands drive rad-hard electronics

By John McHale, Editorial Director

Increased ISR and communications bandwidth demands for military satellites are forcing rad-hard electronics designers to pack more and more performance into smaller form factors. Meanwhile, uncertainty reigns in terms of funding for space-based programs out of the DoD and NASA.



The Lockheed Martin Advanced EHF satellite uses BAE Systems rad-hard boards – 8 RAD750s for the payload and 2 RAD6000s on the bus.

Battlefield success or success in any endeavor for that matter often is dependent on who has the best intelligence. Even as the U.S. military starts scaling back troop deployments in the Middle East, they will continue to increase their Intelligence, Surveillance, and Reconnaissance (ISR) operations to stay one step ahead of enemies and even allies.

Powerful ISR payloads enabled by the supercomputing performance of modern processors and computers are being developed and deployed in manned and unmanned ground, sea, air, and especially space platforms. All of these platforms have requirements demanding more and more performance with less power in ever-shrinking footprints, but the environmental challenges of space add difficulty as each component must be sufficiently radiation hardened, or *rad hard,* to survive for decades.

"Military space customers are facing pressures similar to commercial customers when it comes to performance requirements," says Ken O'Neill, Director of Space Marketing at Microsemi SOC Products Group in San Jose, CA. "Systems need ICs to have higher functionality and higher performance without consuming excessive power. They essentially want to have more functionality in less space.

There is demand for more processing, more bandwidth, and more memory for increased on-orbit storage, says Chuck Tabbert, Vice President of Sales and Marketing at Ultra Communications in Vista, CA. The increased performance requirements will be realized by making use of advanced FPGAs and multicore processors. There also seems to be a strong road map for increasing processing bandwidth by moving more toward fiber-optic technology, Tabbert says. "We are getting requests from customers for 40 Gb box-to-box connectivity over fiber because you can't move that kind of bandwidth over copper." Tabbert's company designs fiber-optic rad-hard transceivers and just patented a rad-hard 40 Gb transceiver.

"The advanced technologies are driving our creativity when it comes to managing all the heat and power they generate as we jam more and more performance into 5- and 10-pound bags," says Tony Jordan, Director of Standard Products at Aeroflex Colorado Springs in Colorado Springs, CO. "Satellite weight has always been [an] issue. Every pound is tens of thousands of dollars of boost launch cost."

"Payload performance demands drive most of the technological change in satellites today," says Peter Milliken, Director of Semi-Custom Products at Aeroflex Colorado Springs. Applications such as signals intelligence and visual imaging are where the technology is going, he adds.

"There is increased pressure on all programs to deliver to the field new technology and on time. However, the debt problem worldwide is restricting satellite growth," Jordan says. "If not for the debt, the bandwidth demand would

be insatiable. Governments and satellite designers want to bring more capability to bear for satellite payloads, transponders, radios, and add features with the capability for remote sensing to have constant 'eyes in the sky.' While I cannot comment on classified programs, they continue to drive technology and are probably under less funding pressure, as they are not as visible as unclassified programs," he adds.

A great example of a Department of Defense (DoD) satellite using existing and new technologies together is the Lockheed Martin Advanced EHF satellite, which "uses eight RAD750s (Figure 1) for the payload with two RAD6000s used on the bus," says Vic Scuderi, Manager of Satellite Electronics for BAE Systems in Manassas, VA. It is a more conservative satellite design that takes a stable bus architecture and marries it with a newer generation payload. The RAD6000 adds stability at the bus level, while the RAD750 provides the necessary processing horsepower for the demanding payload requirements.

There are military space programs (tactical programs, short response time programs) needing parts that combine reprogrammability and high functionality with sufficient radiation tolerance for the mission (usually short duration and Low Earth Orbit), O'Neill continues. "Shorter missions have lesser radiation requirements. Our RTAX-DSP parts are seeing adoption in systems [that] need the additional signal processing horsepower afforded by built-in radiation tolerant multiply-accumulate blocks. The blocks provide higher density, giving users built-in DSP capability in the FPGA to perform signal-processing functions such as Fast Fourier Transforms (FFTs) more efficiently."

There also seems to be a big thrust toward affordability, to scale back some of the requirements to be more cost efficient without compromising reliability, Tabbert says. There might be times where integrators will take a little risk to lower costs, he adds.

Reliability still important

While many terrestrial programs leverage commercial technology right off the shelf, designers of space systems do not often have that luxury. Unlike in a ground vehicle or aircraft, electronic components that are used for satellite control must work for 15 years without failing – as satellites can't go back "to port" for maintenance. Suppliers must be able to demonstrate to government customers that they have the legacy and stability in producing rad-hard electronics, as they will need to support programs that last for decades.

Figure 1 | RAD750 single board computers from BAE Systems come in 3U and 6U form factors.

BAE Systems to develop Freescale QorIQ technology for space

Engineers at BAE Systems in Manassas, VA, have licensed processing technology from Freescale for use in radiation-hardened computers for space.

"We've licensed IP from Freescale" – Power Architecture, the QorIQ platform System-on-Chip (SoC) – as a follow-on to the RAD750, says David Rea, Product Manager at BAE Systems. "The QorIQ platform is compatible from a software perspective with the RAD6000 and RAD750. We will build the QorIQ platform processors at the 45 nanometer level."

According to a BAE Systems release, the Freescale technology will increase onboard satellite processing by as much as 10 times the current rate, enabling new payload and bus applications that were unthinkable in years past. The QorIQ platform includes features such as CoreNet and OCeaN fabrics, memory elements, memory controller, and high-speed interfaces.

"Power management is important for us, and we will take advantage of the inherent power savings of the QorIQ platform and add even more power management features," Rea continues. "Hardening the device typically is a two-year process. We started the process in the middle of last year and expect to have a qualified product by the middle of 2014. The power tweaks will be added at the circuit level as BAE Systems hardens the Freescale IP for high-radiation environments. We harden the device using Rad-Hard by Design techniques. We have 150 nanometers in our fab in Manassas, VA, and relationships with IBM foundries at 90 and 45 nanometers," Rea says. "The IBM foundries are located in Burlington, VT and East Fishkill, NY."

Sidebar 1 | BAE takes QorIQ into space.

Figure 2 | The UT90nHBD ASIC from Aeroflex Colorado Springs is payload centric with strong radiation immunity.

"High performance components are meeting the payload needs but do not need to be as durable as satellite Command Data and Handling (CD&H) electronics, which keep the satellite on orbit," Milliken says. "CD&H devices require more radiation immunity than typically comes in an ASIC technology such as our UT90nHBD, which is payload centric (Figure 2). We also continue to still sell 5-volt technology that is used in legacy platforms of our aerospace and defense customers."

BAE Systems products typically work without ground prevention for as long as 15 years because they are designed to be rad hard from the ground up, Scuderi says. "Integrators that decide to go with commercial products and upscreen them to be rad hard are taking a risk when it comes to reliability. While the importance of flight heritage cannot be overemphasized, higher-performance payload applications demand higher processing and throughput. Our government customers are mindful of the need to mature this technology for space. Our processor technology road map has been funded to develop newer technologies with smaller and smaller feature sizes that translate directly to lower power and higher MIPS [Millions of Instructions Per Second]. Our newest 45 nanometer technology is a good example of this trend." For more on BAE Systems' rad-hard components, see Sidebar 1.

"Our hybrid DC/DC converter and filter customers are increasingly requiring a more complete capability in the components they procure," says Matthew Twitchell, Product Manager – Interpoint Space at Crane Aerospace & Electronics in Everett, WA. "The military space and commercial space markets have shifted from a narrow list of radiation requirements to requiring guarantees in several areas relating to radiation or a summation of effects. Some of these areas include analysis and measured test results for lower dose rates, which are more representative of the space environment – single event upsets, proton fluence, and some higher total radiation doses. These requirements drive the design methods and technologies used in creating the latest products as well as the need to conduct further testing and analysis for existing offerings."

"The design trend overall is moving toward higher levels of integration, including the use of radiation-guaranteed ICs and inherently rad-hard device technologies, such as SiC, SOI [Silicon on Insulator], and GaN," says Jay Kuehny, Principal Engineer, Crane Aerospace & Electronics. "While higher levels of integration serve lower cost and higher densities, great care must be taken to ensure robustness to single event effects. This often includes long design and qualification cycles and can result in high levels of redundancy, ultimately driving a more costly solution. To support the growing trend of longer-life spacecraft, these ICs must also be available to support program durations measured in decades rather than years. With the military and space markets extending program life expectations and the desire for proven technology, we have noted a slower rate of adoption for newer designs."

Crane's latest Interpoint converter product is the MFP Series point-of-load converter, Twitchell says. This device is guaranteed to 100 krad total radiation dose, Enhanced Low Dosed Radiation Susceptibility (ELDRS) level of 30 krad, to an LET of 85MeV-cm^2/mg for single event effects and is Space Qualified to Class K per MIL-PRF-38534 on a Defense

Logistics Agency's (DLA's) Standard Microcircuit Drawing (SMD) number.

Other rad-hard offerings

VPT engineers have added a 15 A point-of-load DC-DC converter to their family of power conversion products for space applications. The SVGA0515 Series is a non-isolated, regulated buck converter, which steps down the voltage at the point of use in a distributed power system. It is qualified to MIL-PRF-38534 Class H and Class K by the Defense Logistics Agency and is targeted for power systems used on GEO, MEO, LEO, and deep-space applications.

The latest rad-hard FPGA offering from Xilinx is the Virtex-5QV FPGA, built on the second-generation ASMBLTM column-based architecture of the Virtex-5 FPGA family. It has protection from Single Event Upsets (SEUs), Single Event Transients (SETs), Single Event Latchup (SEL), and high Total Ionizing Dose (TID) – 1Mrad (Si). The device has 131,072 logic cells, is an integrated high-speed SERDES solution for space, and has 18 channels of >3 GHz multi-gigabit serial transceivers enabling high bandwidth for chip-to-chip, board-to-board, and box-to-box communications. For more rad-hard suppliers, see Sidebar 2.

Funding for space

Despite the increasing demands for performance on the payloads, funding for space programs from the DoD and other government agencies remains uncertain or flat at best for the next few years.

"What we're observing in the U.S. DoD market is a lot of uncertainty about when funding for procurement will be released, which makes it harder to forecast business," O'Neill says. "The uncertainty also causes hesitation on the contractor's part when releasing purchase orders. However, design activity seems to be relatively unaffected and remains constant with substantial activity going on in various programs."

"DoD funding trends have generally slowed many existing space programs [that] were previously very active in the procurement phase," Twitchell says. "This has translated into some shifting in the timing but has not yet materialized into cancelations. Recent DoD funding shifts have influenced the market by slowing the expected growth rates with our traditional customers. While the medium- to short-term growth rates seem to have flattened, it is expected that the commercial market and new partners in the space arena will begin to increase demand for space-qualified components. While this trend or shift to the commercial approach looks promising, the requirements for testing, analysis, and guarantees for product performance continue to increase. These [three] factors in combination look to provide us a very interesting next few years in the space market."

"DoD budgets are not yet beginning to slow on programs, because procurement for programs to be released in 2012, 2013 has been completed already," says Minal Sawant, Segment Marketing Manager at Microsemi. "The effects of budget cuts will be seen in 2014 and beyond, since programs are being put on hold."

"Budget cuts have impacted DoD and NASA missions, but we are fortunate that our business model includes a strong mix of commercial satellite opportunities as well," Twitchell says. "The commercial market has been holding steady across the international scene, and we have benefitted from this stability. Secondary payloads for DoD applications will also pave the way for government and commercial satellite ventures that are able to bring newer technologies into space." **MES**

Rad-hard company listings

Aeroflex Colorado Springs
www.aeroflex.com/radhard

Aitech
www.rugged.com

Aldec
www.aldec.com

Atmel
www.atmel.com

BAE Systems
www.baesystems.com

C-MAC MicroTechnology
www.cmacapi.com

Corwil Technology Corp.
www.corwil.com

Crane Aerospace & Electronics
www.interpoint.com

Curtiss-Wright Controls Defense Solutions
www.cwcdefense.com

Harris
www.harris.com

Honeywell Microelectronics
www.honeywellmicroelectronics.com

Integra Technologies
www.integra-tech.com

International Rectifier
www.irf.com

Intersil Corp.
www.intersil.com

Jaz Semiconductor
www.jazzsemi.com

Linear Technology Corp.
www.linear.com

Maxwell Technologies
www.maxwell.com

Microelectronics Research Development Corp.
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Micropac Industries
www.micropac.com

Microsemi
www.microsemi.com

Modular Devices
www.mdipower.com

MS Kennedy
www.mskennedy.com

Novocell Semiconductor
www.novocellsemi.com

Peregrine Semiconductor Corp.
www.psemi.com

Ridgetop Group
www.ridgetopgroup.com

Robust Chip, Inc.
www.robustchip.com

Rochester Electronics
www.rocelec.com

Semicoa
www.semicoa.com

Silicon Space Technology
www.siliconspacetech.com

Silvaco
www.silvaco.com/government/index.html

STMicroelectronics
www.st.com

Synopsys
www.synopsys.com

Synova
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Teledyne Microelectronic Technologies
www.teledynemicro.com

Texas Instruments
www.ti.com/home_p_hirel

TRAD
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Triad Semiconductor
www.triadsemi.com

Ultra Communications
www.ultracomm-inc.com

VPT
www.vpt-inc.com

Xilinx
www.xilinx.com

Sidebar 2 | Many companies are supplying rad-hard space electronics.

Rad-hard SRAM FPGAs enable vast improvements in space exploration

By John D. Corbett and Gary M. Swift

As purpose-built Radiation Hard (RH) ASICs fall farther and farther behind in device technology and with their associated development costs and risks spiraling out of control, SRAM-based FPGAs present an ever-more attractive alternative for space applications and systems, also beating out traditional microprocessors and microcontrollers, DSPs, or One-Time Programmable (OTP) FPGAs.

Photo by NASA

Space environments have high levels of ionizing radiation that create complex design challenges for military systems engineers. Thus, electronic systems used in space must have circuitry that is highly reliable and able to endure extreme amounts of radiation. In space, it isn't a matter of if electronics will encounter radiation but how much, how often, and how will the device deal with each exposure to radiation. A single charged particle in space can knock thousands of electrons loose, causing electronic noise and signal spikes that can, if unchecked, cause systems to malfunction.

While design and system-level mitigation can ensure the proper operation of military spacecraft and instruments, high reliability and high availability are much easier to achieve with Radiation Hard (RH) components. High reliability is especially critical in systems such as the processing circuitry that runs command and control – the telecommunications system in charge of telemetry to and from ground control where a failure can jeopardize the entire mission. Increasingly, government and private agencies deploying spacecraft are turning to SRAM-based FPGAs to perform these vital processing tasks because their capabilities have dramatically outpaced the traditional custom ASIC or One-Time Programmable (OTP) FPGA approaches.

Rad-hard SRAM-based FPGAs are giving space system designers a compelling set of performance, feature, and flexibility advantages for their new projects. The all-programmable nature of SRAM-based FPGAs enables the capabilities of a system to be improved and expanded even after launch when physical access is no longer possible. The hardware-programmable nature of FPGAs makes them even more flexible than stand-alone processors such as microprocessors, DSPs, and microcontrollers that are only software programmable. What's more, the largest FPGAs can provide the function of multiple processors and other devices, all on a single chip.

Currently two types of FPGAs are used in space applications: anti-fuse-based one-time programmable FPGAs and SRAM-based reprogrammable FPGAs. Each type of device has its advantages and disadvantages. The anti-fuse-based devices have fewer programmable elements and thus fewer elements that can be upset by radiation. In addition, space-grade anti-fuse devices make extensive use of redundant circuitry. Their relative simplicity and familiarity provide reassurance to space system designers and project managers.

However, like RH ASICs, anti-fuse devices are not available in smaller process geometries such as 90 nm or 65 nm and thus have much lower capacity and performance than SRAM-based devices. SRAM-based devices enjoy a multiple-generation advantage in process geometry, thus offering greater capacity and performance, while consuming less power per gate. SRAM-based devices require configuration each time they are powered-on, and radiation-tolerant, SRAM-based devices may require more extensive error mitigation in the design implementation, such as adding Triple Modular Redundancy (TMR) or error correcting codes.

On the flip side, upset mitigation can be applied selectively where most needed in a reconfigurable FPGA (versus a nonreconfigurable OTP FPGA approach), thus making better use of resources. While configuration at startup adds complexity to the system, it also adds flexibility; last-minute requirement changes and bug fixes can be accommodated even when shortcomings are not apparent until after launch. The Virtex-5QV FPGA reduces the complexity of error mitigation in SRAM-based FPGAs by replacing the traditional 6-transistor configuration memory cell with a rad-hard-by-design, 12-transistor cell that is about 1,000x harder to upset than commercial SRAM cells. Thus, SRAM-based FPGAs are useful in myriad space applications (See Sidebar 1 and also Figure 1).

FPGAs conquer another frontier

It's difficult to overstate the value an FPGA can offer in a space-bound system application. Once deployed, there is little or no ability to make hands-on hardware changes, so the programmability of an SRAM-based FPGA is a huge benefit. To be sure, microprocessors and microcontrollers can also be reprogrammed. But FPGAs excel in data-flow applications where functions such as packet inspection or signal-processing algorithms implemented in hardware logic offer far more processing throughput than traditional microprocessors. And the FPGA hardware can be easily reconfigured to support new algorithms.

To deploy FPGAs in space applications, however, designers have to understand the environment and learn how to mitigate issues that affect reliability.

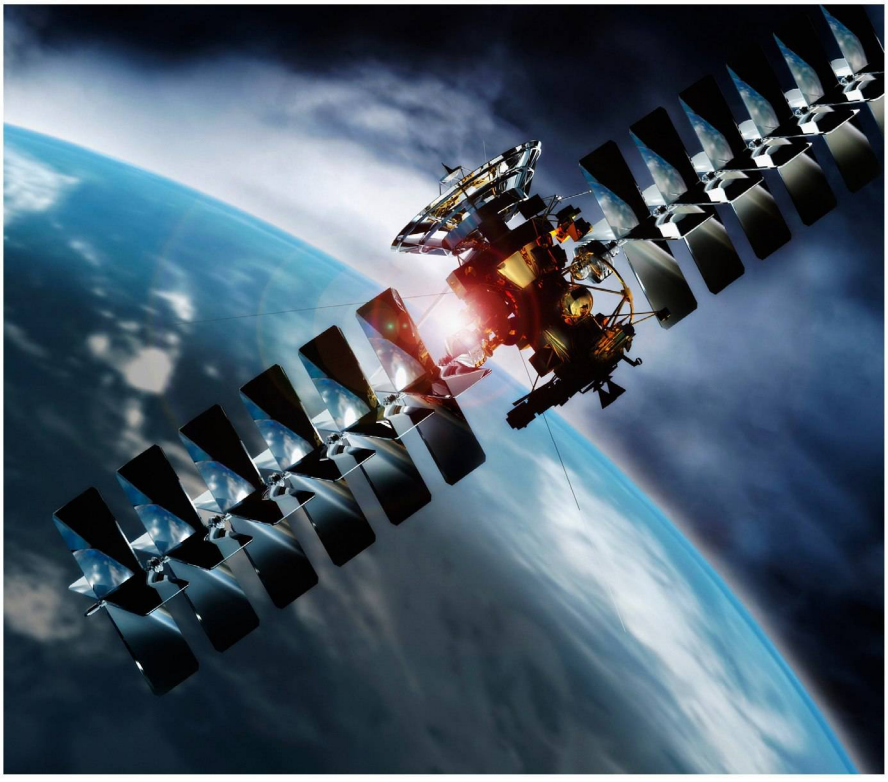


Figure 1 | FPGAs have proven useful in many space applications.

Upset hardening in hardware

SRAM-based FPGAs are now offered as fully radiation-hard components. That reduces or eliminates the need to use TMR in space designs and thus frees up space on the FPGA for design teams to integrate more functions with lower payload weight, power consumption, and system cost while improving functionality and sophistication of their systems.

To create these radiation-hard SRAM-based FPGA devices, a variety of techniques is used to implement the underlying FPGA memory and circuit elements in the device. Hardening the 35 million configuration cells and the 81,920 user flip-flops was accomplished with a self-redundant storage circuit that has double the typical number of transistors. The result is that susceptibility to SEU in space radiation environments was improved by 1,000x validating the circuit choice and the optimization of its layout, which involved fabricating many variants and subjecting them to in-beam irradiation tests.

In addition, all the clock, data, and asynchronous inputs to the flip-flops are protected with programmable filters to suppress single-event transients. Internal control circuitry was upset hardened to reduce troublesome SEFIs by 100x to practically zero where "practically zero" is defined as an expected rate of less often than once every 10,000 years.

Consequentially, design teams can now use SRAM-based FPGAs that are fully characterized for space radiation effects in heavy ion and proton environments and will withstand a TID of 1,000 krad(Si), guaranteed based on Test Method 1019 as defined in MIL-STD-833. That's more than triple the TID rating of radiation-tolerant OTP or typical SRAM-based FPGAs.

Sidebar 1 | To be useful in space applications, FPGAs must be radiation hardened.

A number of radiation-induced effects have been identified as a problem area for space-based designs:

- Single Event Upsets (SEUs)
- Single Event Transients (SETs)
- Single Event Functional Interrupts (SEFIs)
- Single Event Latchups (SELs)
- Total Ionizing Dose (TID)

Of the radiation effects listed here, the latter two are particularly troublesome because they are destructive; consequently, space engineers require components with proven SEL immunity and large TID margins (2x or 3x) to cover extreme space weather they might encounter. The other three single-event effects might cause temporary malfunctions with varying seriousness depending on the application, ranging from none through annoying all the way to mission loss. SEFIs, though exceedingly rare, can be troublesome: Although recovery may take less than a second, it does require reconfiguring the FPGA with a resultant design outage. Thus, SEFI elimination is highly desirable. Somewhere in the equation, the terms *rad hard* versus *radiation tolerant* play a role (see Sidebar 2).

Defining terms: 'Rad hard' versus 'radiation tolerant'

Experts will disagree on exactly what thresholds a *radiation-hard* part must meet, but get strict enough and agreement emerges: A device that meets (1) one mega-rad of dose, (2) exhibits immunity from single-event destructive effects, and (3) upsets at a rate of no more than 1×10^{-10} per bit-day in GEO is almost universally considered *rad hard.*

Radiation-tolerance is bit harder to define. In the most prevalent usage, it means that the radiation tolerance levels (whatever they are – maybe they are quite low) are known and, perhaps, guaranteed – at least some of them. Finally, *radiation hardened* is an adjective that manufacturers use to indicate that they intentionally did something to improve at least one radiation characteristic.

Sidebar 2 | "Rad hard" versus "radiation tolerant" explained

Defining terms: 'Rad hard' versus 'radiation tolerant'

In essence, the radiation-hard SRAM-based FPGA has special circuitry to practically eliminate SEUs and SETs. Older SRAM-based FPGAs do not, but they do have error detection hardware that can be used in combination with soft TMR to practically mitigate the effects of SEUs and SETs (see Sidebar 3). The older approach is more complicated for the system designer.

Boldly going where none have before ...

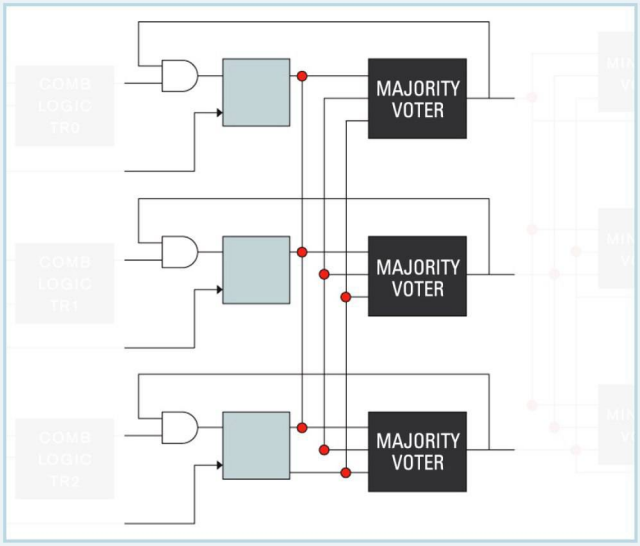
Design teams creating systems for space applications are finding that

Radiation tolerance and Triple Modular Redundancy

In the past, designers wanting to use FPGAs have had to combine radiation-tolerant ICs with techniques that further mitigate SEU effects. Typically design teams have employed Triple Modular Redundancy, a commonly known method for SEU mitigation with voting that enables designs that are robust and therefore protected from upsets from radiation strikes because there are no single points of failure (see Sidebar Figure 1). In a TMR design, teams create three separate instantiations of their system in three separate devices or in a single FPGA. As SEUs are relatively rare (generally 1 to 30 per day), extremely high reliability can be achieved by majority voting combined with fixing configuration upsets as they occur, which can be done without interrupting the design's normal operation.

In anti-fuse-based FPGAs, TMR is applied to every D-type flip-flop and a voter is added on its output. While this greatly improves SEU resistance, errors will accumulate over time unless the output of the majority voter is used to correct any flip-flop that gets upset. The accumulation of errors degrades the effectiveness of any redundancy scheme.

FPGA vendors and even commercial EDA tool vendors such as Mentor Graphics and Synopsys offer TMR automation software that handles the error-prone work of triplicating the design. TMR design automation can greatly accelerate the design cycle by allowing the design team to focus on functionality and debug rather than TMR. The Xilinx TMRTool software works seamlessly with any HDL and synthesis tool to automatically build TMR into a design. It also goes beyond baseline TMR functionality. It triplicates all clocks and throughput logic to protect against SETs. It inserts majority voters on all feedback paths, thus preventing errors from accumulating.



Sidebar Figure 1 | Triple Modular Redundancy with voting

By inserting voters on all feedback paths, a TMR tool overcomes a problem with the technology in designs with finite state machines: In most TMR-based state machine designs, an SEU that causes an error in one of the three state machines ultimately requires that the state machines be reset for synchronization. But the voters in feedback paths ensure that the state machines are not only voted for error-free output in the presence of SEUs and SETs, but that correct output is used for feedback to resynchronize all of the internal, triplicated state elements. TMR within a single-chip synchronous design elegantly avoids problems associated with synchronizing the processing of multiple redundant chips.

Sidebar 3 | Typically design teams have employed Triple Modular Redundancy, a commonly known method for SEU mitigation.

FPGAs offer numerous advantages over other devices. The hardware and software reprogrammability of SRAM-based FPGAs, zero manufacturing NRE, and vast capacity make these FPGAs extremely attractive for a growing number of space applications. For example, NASA's highly successful Mars rovers Spirit and Opportunity used SRAM-based reprogrammable FPGAs for critical functions like pyrotechnic firing sequencing during landing and wheel motor control during roving. Using TMR with radiation tolerant SRAM-based FPGAs has allowed design teams to create some amazing systems that are extremely reliable. Now new radiation-hardened SRAM-based FPGAs will allow them to achieve even more remarkable feats and boldly go where no one has gone before. **MES**

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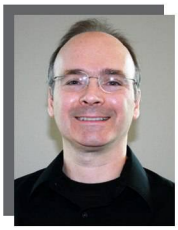

John D. Corbett *is a Staff Software Engineer at Xilinx with more than 20 years of experience developing CAD tools for user interface design, education, architecture, computer security, and fault tolerance. At Xilinx, he developed software used to verify Xilinx FPGA designs are suitable for use in Type I cryptographic systems. Prior to Xilinx, he worked at Xerox PARC, Silicon Graphics, and several small startups. John holds seven patents and obtained a BS in Math/Computer Science from Carnegie Mellon.*

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Implementing analog functions in rugged and rad-hard FPGAs

By Allan Chin and Luciano Zoso

All-digital chips such as FPGAs have traditionally not been able to house analog blocks like ADCs, clocking functions, or power converters. Now, aerospace engineers are pulling some of these analog functions onboard FPGAs to take advantage of rugged and radiation-hardened properties.

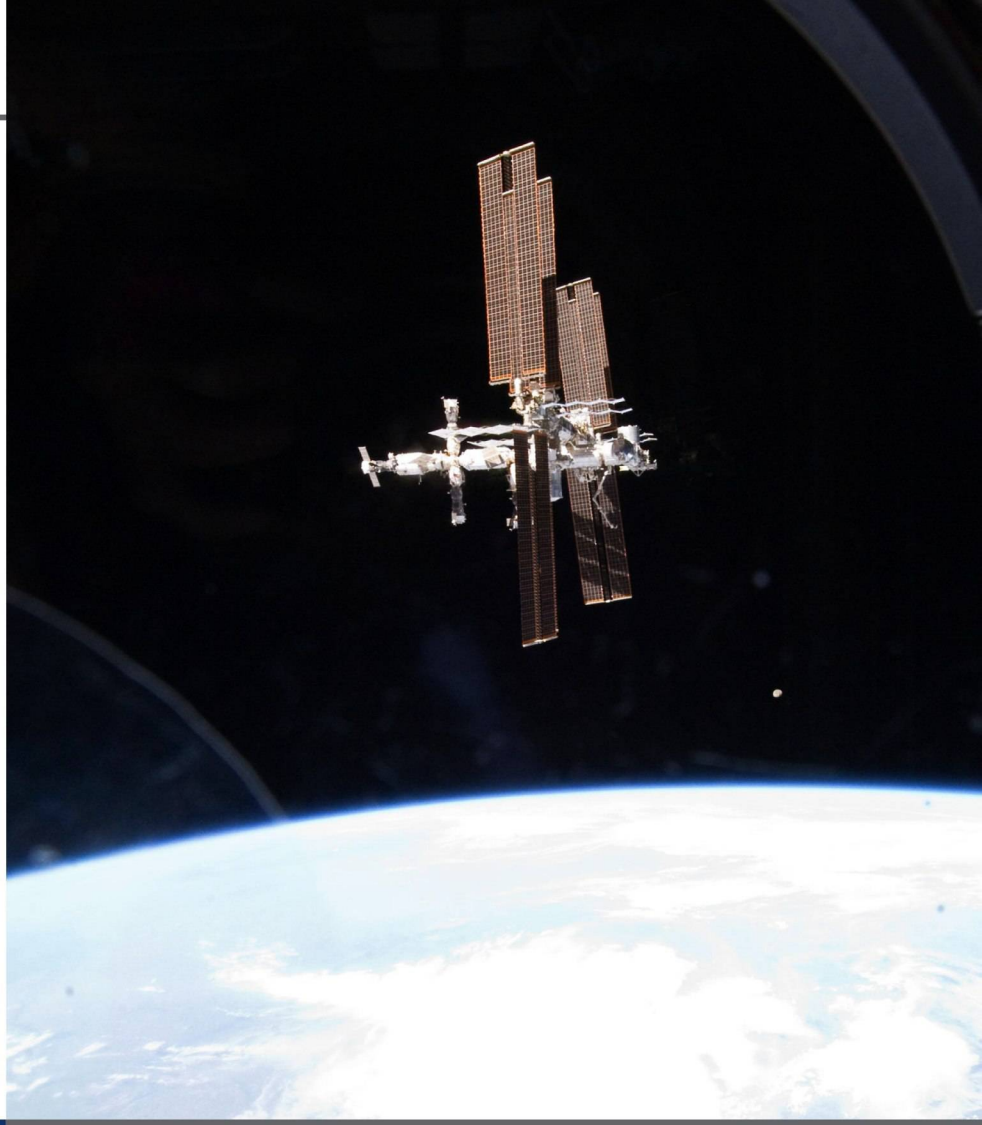

Photo by NASA

FPGAs are transforming systems engineering for high-reliability applications. FPGAs changed the cost/reliability paradigm for embedded systems in high-reliability applications with advances in hardness and power reduction. Still challenges exist. On many embedded applications for high-reliability systems, a number of peripheral analog components such as ADCs and DACs are relied on to talk to the real world. Other system components such as PLLs and DC-DC converters are usually required to complete a system design. These peripherals impact overall cost, size, and reliability. Peripheral analog parts can also be challenging to work with and to source for radiation environments, as an example. However, to further leverage the power of FPGAs, mil/aero engineers are actively looking for ways to integrate many of these analog functions onto the FPGA. Synthesizable, digital IP cores to replace some analog functions now exist, which allow ADC, DAC, DC-DC controller, and clock multiplier functions to be implemented in fully digital processes such as FPGAs. This new ability leverages the advantages of FPGAs and helps mitigate many challenges of using analog components in high-reliability applications.

Overcoming high-reliability design challenges

Challenges to engineering for military or high-reliability applications such as aerospace are numerous. Power and weight are usually under strict budgets because they can affect operating costs and insertion costs exponentially. Physical shock, force survival, and SEU and latchup protection often mean that parts are larger, heavier, and more power hungry than commercial parts. For instance, a commercial 12-bit, 10 MHz bandwidth ADC is approx .71" by .42" and consumes 280 mW power. The equivalent radiation-hard part is .81" by .72" and consumes 335 mW power. That's almost double the size and 20 percent more power.

Wide temperature range is another issue. Typically, temperatures of -40 °C to +80 °C are expected for many military embedded applications here on Earth. Temperature takes on another complexion in space. In satellite electronics design, for instance, normal operating junction temperature might be -55 °C to +125 °C. Monitoring this onboard temperature is key to effective system maintenance, but adding a radiation-hard ADC part to provide this function can add up to one square inch of board and require additional components and testing.

When a high-reliability design relies on peripherals such as ADCs, DACs, DC-DC converters, or PLLs, each one of those components represents a possible point of failure. Each must be qualified and tested, and each is most likely not optimally designed for the specific need. There is also always a risk that the manufacturer discontinues the part, forcing requalification of the entire system.

These challenges to working with analog components in high-reliability environments can now be mitigated by using the FPGA. This new paradigm is explored next.

Pulling analog functions onto the FPGA

Regardless of how "analog" and "digital" are defined, significant differences and integration issues exist between the two. Because of these issues, it can be very advantageous to have digital designers pull analog functions onto an FPGA and test them. Herein, "digital" is defined as using standard digital library cells and passive components for a fully synthesizable and digitally testable design. Digital IP blocks of ADCs, DACs, DC-DC converter controllers, and clock multipliers can be created in RTL format and implemented in all digital processes.

With these IP blocks, military designers can take advantage of rugged and radiation-hardened FPGAs to implement customized analog functions within the FPGA. Not only does this take advantage of the inherent protection properties of the FPGA, but these blocks are also a great way to utilize unused FPGA resources. Xilinx and Microsemi recognize this advantage and now partner with companies like Stellamar to provide these functions. Increasingly, aerospace companies are turning to these solutions to attack analog integration problems.

Digital ADC cores yield benefits

Figure 1 depicts an example block diagram of the Digital ADC IP core. With the digital approach, Digital ADC IP cores require only a few external passive components. IP core is instantiated right in the FPGA and is much easier to implement through digital synthesis. On a Xilinx Virtex-5QV, a scenario such as that pictured in Figure 1 utilizes less than 1 percent of FPGA resources.

Proprietary signal processing enables analog sigma-delta ADC performance to be replicated with all digital library cells. Companies like SEAKR Engineering and the Finnish Meteorological Institute are using Digital ADC IP in their On Board Processor Program and Lunar Landing Missions, respectively. Some benefits are:

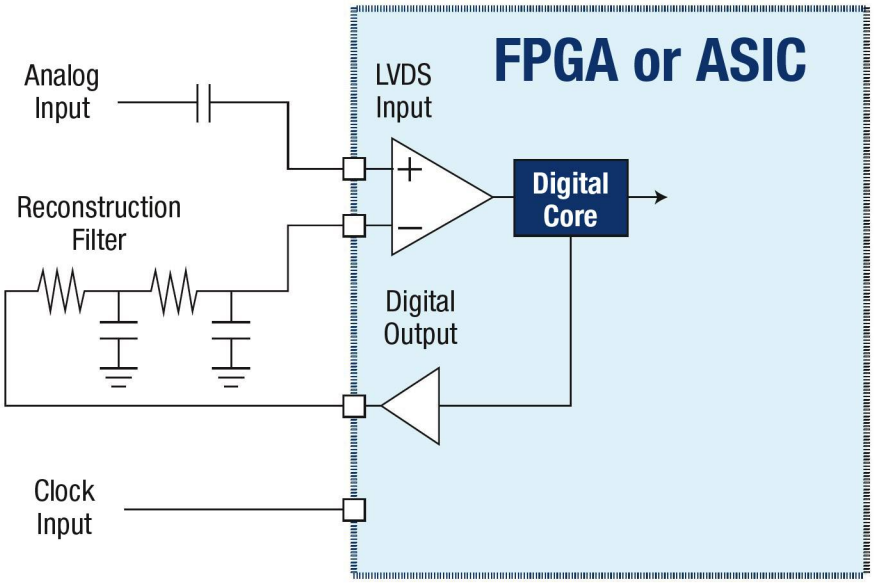

Figure 1 | An example of an all Digital ADC IP core interface

- 50 percent lower power than analog ADC parts
- 68 percent smaller area than analog ADC parts
- Process technology independence
- Reduced risk and cycle time
- Digital integration, synthesis, and testing
- Easier radiation-hardened design

Performance + applications

Current performance is up to 14 bits of resolution and 100 KHz bandwidth. Bandwidth depends on the selected resolution. Current performance is suitable for a host of applications including:

- Sensors – temperature, pressure, voltage, current, and acceleration
- Touch-screen integration
- Voice and high-quality voice
- Motor control

As an example, many design teams use the radiation-hardened, 12-bit, 10 MHz bandwidth ADC part mentioned in the Design Challenges section for monitoring onboard temperature and voltage. Some FPGAs, such as the Xilinx Virtex-5QV Space Grade FPGA even have embedded diodes highlighting the importance of the temperature-sensing function. However, normal bandwidths for these types of measurements are 0.5 Hz to 10 Hz, so using bandwidth in the MHz is like driving the head of a pin with a sledgehammer. A Digital ADC IP core on a radiation-hardened FPGA can get down to 0.5 Hz bandwidth per channel and consume less than 6 mW power versus 335 mW power for the external part. Why waste critical board space and power for such a low-level task?

DC-DC power management control onboard FPGAs

Power management is becoming a larger part of overall system design. Sometimes a single design can include more than 30 power supplies. External radiation-hardened DC-DC converters retain the same difficulties as external ADCs, as described earlier. Thus, the use of these parts to control power complexity in high-reliability applications does not scale well. All-digital DC-DC controller IP now exists to take advantage of radiation-hardened FPGAs' processes and to allow for simplification of control, redundant power

supplies, infinite sequencing, and infinite throttling. An external power transistor is needed, but this can be much easier to work with than a full DC-DC converter part.

Digital clocking solutions

PLLs are some of the most widely used analog blocks for clock generation; thus, most FPGAs have incorporated PLL capability within the package. However, some FPGAs including some radiation-hardened FPGA families do not include PLLs at all. Other radiation-hardened FPGAs generally do not include the PLLs in the radiation-hardened portion of the package.

Digital clock multiplier IP can be used on these FPGAs and can provide the ability to generate any clock up to about 2 GHz with no lock time. Models show 50 ps peak and 35 ps RMS and 5 to 1 ns rise/fall. As with Digital ADC IP, very few off-the-shelf passive components are required.

Putting it together

Historically, FPGAs did not lend advantages to analog functions, forcing high-reliability design teams to use nonoptimal external analog parts. This is no longer the case, as mil/aero engineers now have robust options for integrating analog functions into any digital fabric, including radiation-hardened FPGAs. By using digital implementations of analog functions from Stellamar, engineers can add critical functionality like thermal monitoring, redundant power supplies, and clocking functions – all without adding weight, power, or size to the design. The digital synthesis and test methodology ensure the operability and greatly increase reliability. Further, these technologies can be leveraged across projects and the whole organization easily. With budgets being slashed and performance more important than ever, these digital IPs give mil/aero engineering teams the flexibility and productivity needed to meet critical mission objectives. **MES**

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Floating-point coprocessors enable FPGAs to replace DSPs

By Jeff Milrod

A coprocessor can greatly improve the productivity and algorithmic flexibility of an FPGA, thereby enabling it to handle a larger part of a signal processing implementation.

U.S. Navy photo by Mass Communication Specialist 3rd Class Nicholas Hall

Using FPGAs for embedded military computing isn't a new idea. Wikipedia calls it "reconfigurable computing" and traces it back to the 1960s. In theory, tailored hardware runs faster and uses less power than programmable CPUs, hence greatly improving Size, Weight, and Power (SWaP). Academics have thoroughly tested this idea. Adopters have shipped it. The reviews are in and they are mixed. FPGA computing sometimes falls short in practice. However, FPGA computing can be successful now, and that success can be extended with floating-point coprocessors that enable FPGAs to replace DSPs.

FPGAs are great – but not perfect (yet)

Outstanding FPGA success stories indeed exist. What do they have in common?

- The system already contains FPGAs managing real-time I/O.
- That I/O drives computation.

A marriage between I/O and computation describes a large percentage of DSP applications, and indeed FPGAs are frequently used in signal processing applications. But what additional factor is required for the successful deployment of FPGAs?

1. FPGAs computation succeeds when algorithms are "data independent." Put another way, if the algorithm contains few "if" statements or can be expressed as a state machine, FPGA tools can translate that algorithm into efficient Register Transfer Level (RTL, hardware's assembly language).
2. A second key insight is that FPGAs are appropriate platforms when the data-independent algorithm is "mature." This is because expressing computations using gates requires more effort to optimize and to test than the programmable DSP alternative. Thus, to meet development schedules, the algorithm can't be changing with every firmware release.

Identifying when things work well implies things aren't so great in other cases. Using FPGAs is questionable when an algorithm isn't mature (or is ever changing in response to new threats or modes), or if it is "data dependent" (that is, the algorithm changes based upon the specific data flowing through the chip). However, this doesn't mean FPGAs won't evolve to close the gap.

Prior attempts to extend the FPGA

An early solution was to put CPU cores inside an FPGA. This approach began with "soft" cores and extended to include hard cores. In 2002, Xilinx integrated "hard" PowerPC cores.

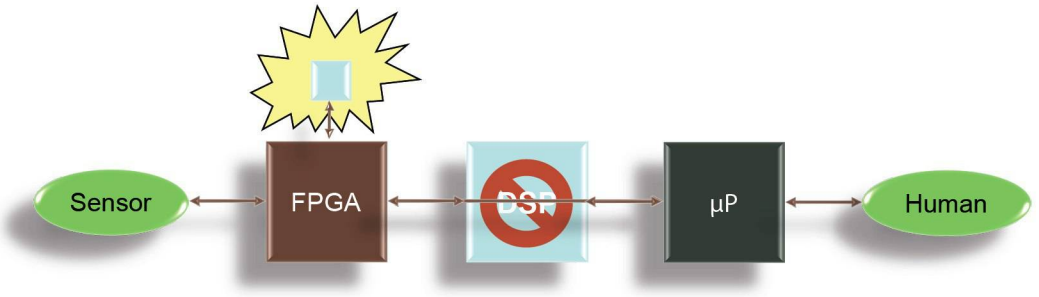


Figure 1 | Adding a coprocessor to the FPGA can eliminate the need for DSPs.

Today industry leaders Altera and Xilinx both offer FPGAs with ARM cores inside. Theoretically, this could close both the maturity and data-dependency gaps.

Unfortunately, integrated cores have only successfully addressed the low end of the data-dependent and maturity challenges. We say "low end" because integrated cores have had narrower feature sets and lower clock speeds than separate DSP and embedded microprocessors. They are simply not powerful enough for most signal processing applications. However, integrated cores are ideal for out-of-band applications, such as hosting a USB protocol stack or controlling the processing of data through the rest of the FPGA.

Another attempt to bridge the gap has been High-Level Synthesis (HLS) tools and C-to-RTL or C-to-gates tools. Conceptually, these tools allow developers to abstract the FPGA or program it in standard C, thereby enabling rapid algorithm changes. In practice this hasn't worked out, since low-level hardware dependencies are legion, and the abstractions and C end up having to depend upon language extensions that significantly deviate from standards and/or generate code that instantiates a runtime architecture that is effectively a soft processing core. Arguably these tools have reduced the gap, but specialized design skills and extensive compiles and simulations are still required. These problems are exacerbated with data dependencies.

A new approach to extend FPGAs

One new idea has potential for simultaneously closing the internal core/signal processing gap and the maturity gap. Rather than embed "low-end" hard or soft cores in the FPGA or try to abstract the FPGA to make it programmable with standard methodology, an external chip full of processing resources could provide standard C language design flows to the FPGA – a coprocessor to the FPGA, so to speak.

Ideally, it would be a highly efficient coprocessor tightly integrated with the FPGA to extend the performance of the FPGA while providing straightforward C programmability. Having it use floating point would further simplify the design and implementation of new and changing algorithms. Leveraging the trend to multicore would bring impressive peak performance numbers and could dramatically lower power consumption – over 30 GFLOPS per watt – making it more effective at addressing embedded military and SWaP demands.

The coprocessor could sit directly on the FPGA fabric, looking to VHDL or Verilog tools just like an embedded soft or hard core. This tight integration would give the coprocessor direct access to data inside the FPGA and allow very fine-grained interaction with the FPGA, and vice versa.

This new approach, a coprocessor for the FPGA, would combine the best of both worlds. It maintains the uncompromised strengths of the FPGA while bridging the maturity and data dependence gaps by leveraging the ease of use and power efficiency of a programmable multicore processor. As shown in Figure 1, such a device extends the capabilities of FPGAs to replace DSPs in many, if not most, embedded signal processing systems.

A new approach to extend FPGAs – Implemented

What should this new coprocessor architecture look like? Perhaps the chip should feature a tiny core optimized for floating-point calculations that is integrated with a high-performance mesh network to allow scalable multicore implementations.

The core isn't a PowerPC or MIPS chip; it is a new instruction set designed for efficiency and coprocessing. One tidbit that may provide understanding of the design trade-offs: The instruction set is built around a floating-point multiple/accumulate instruction (great for DSP); however, it is unusual in not offering an integer multiply instruction. Think no-frills, optimized computing. The result of this tight focus is that each core is tiny and can deliver 800 megaflops in 25 milliwatts, or 32 GFLOPS per watt. By comparison, a wristwatch consumes three times more power and runs for a year off a button battery.

The coprocessor reduces system development cost and directly bridges the FPGA's gaps of requiring algorithmic maturity and data independence, by enabling out-of-the-box execution of applications written in regular ANSI C. It does not use any C subset, language extensions, SIMD, or other "funny stuff." Standard GNU development tools are supported including an optimizing C compiler, simulator, GDB debugger with support for multicore, and an Eclipse multicore IDE.

Higher-level tools and abstractions such as OpenCL, multicore profilers, and optimized libraries further enhance the opportunity for the coprocessor approach to improve productivity.

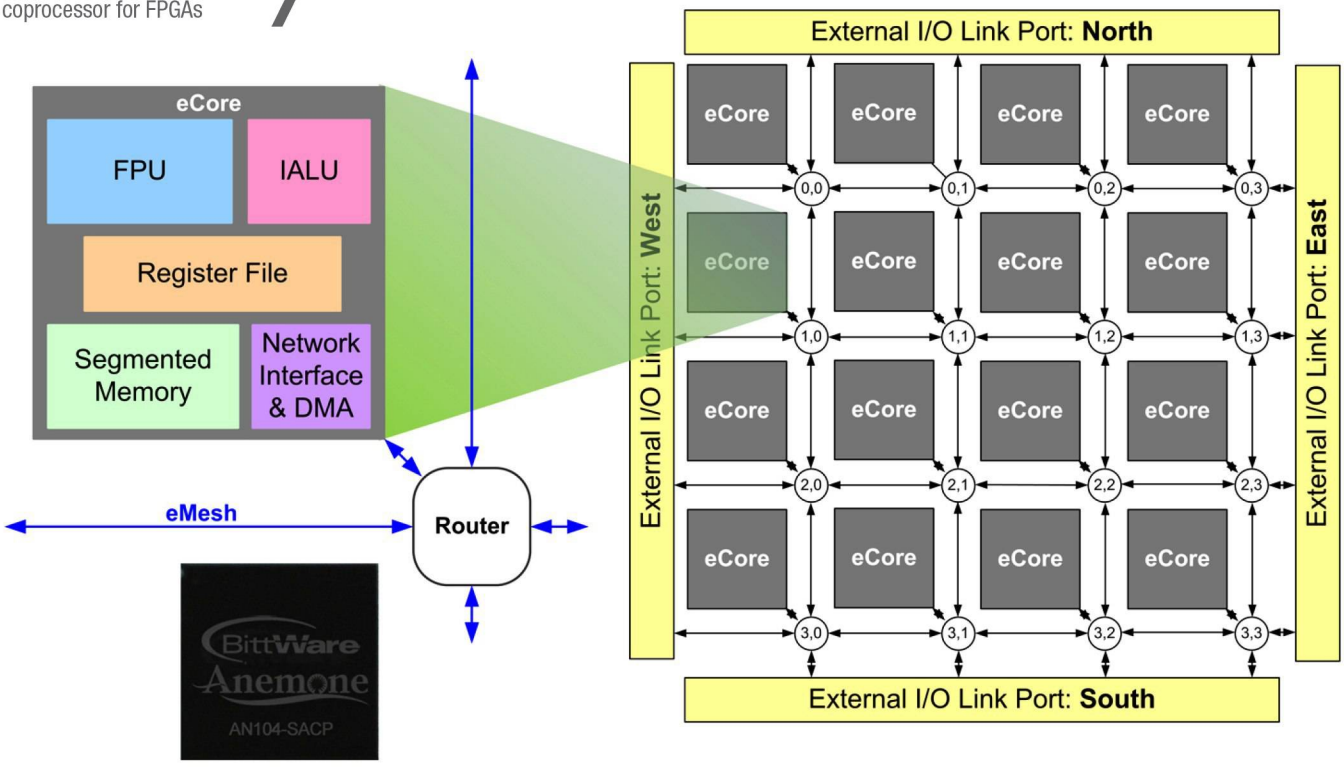
"Think no-frills, optimized computing. The result of this tight focus is that each core is tiny and can deliver 800 megaflops in 25 milliwatts, or 32 GFLOPS per watt. By comparison, a wristwatch consumes three times more power and runs for a year off a button battery."

Seeing the opportunity this new approach provides to users of FPGAs, BittWare partnered with a startup to develop just such a floating-point coprocessor for FPGAs. The resulting chip is the Anemone coprocessor for FPGAs.

The coprocessor uses 16 cores to balance performance with I/O to the FPGA, since fine-grained acceleration of an FPGA is all about data movement and synchronization. If more FLOPS are required, additional coprocessors can be gluelessly added to create seamless arrays of larger core counts (Figure 2). Future generations will boast up to 64 cores each and will deliver 96 GFLOPS of double precision floating-point processing while achieving efficiencies exceeding 50 GFLOPS per watt.

To take make this new approach readily available for COTS military deployments, Anemone is available on an FMC card

Figure 2 | Floating-point coprocessor for FPGAs



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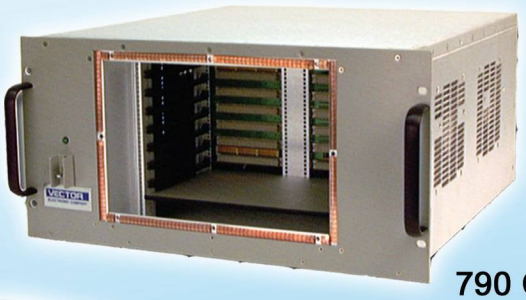

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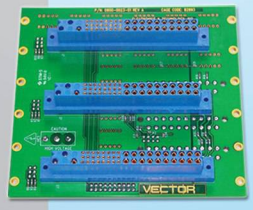

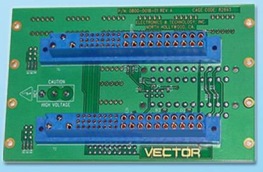

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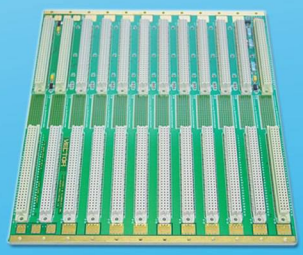

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Secure at the source: Integrating static analysis into the embedded developer's desktop

Presented by: Wind River and Coverity

Security defects that lead to exploitable vulnerabilities are often introduced during design and development either through in-house development or outsourced and other third-party source code, including open source technology. The cost of fixing defects increases dramatically the longer they go undetected, and security defects can become very expensive to fix for products already shipped, up to 100 to 1,000 times more.

The integration of Coverity Static Analysis into Wind River Workbench means defects can be caught right away, before they enter the source code repository. Many of the Common Weakness Enumeration (CWE) Top 25 Most Dangerous Software Errors are detectable via static analysis.

AltiVec unleashed – Bringing unprecedented performance levels to signal processing

Presented by: Mercury Computer Systems and Freescale

Mercury Computer introduces an OpenVPX blade utilizing Freescale's T4240 28nm QorIQ Power Architecture processor that provides 24 virtual cores and 12 AltiVec engines in a single SoC device. Freescale and Mercury will provide technical details of the processor and how Mercury utilizes the raw processing power and performance per watt of the T4240 processor. Performance, bandwidths, and AltiVec performance with Mercury's scientific application libraries will be discussed.

Meeting DO-178 objectives for source code

Presented by: MathWorks

Learn how verification tools can save time for compliance to DO-178 objectives for source code. Embedded software that must comply with DO-178 may consist of automatically generated and/or handwritten code and must satisfy Annex Table A-5 of DO-178 in order to obtain approval of the software by certification authorities. However, achieving DO-178 approval for Levels A, B, and C by meeting objectives for source code is a resource-intensive and time-consuming process. MathWorks engineers will discuss how verification tools can be used to automate and streamline the process in addition to how certification credits can be obtained with verification products from MathWorks.

Adding "Wow" to embedded with next-generation Intel Atom processors

Presented by: Advantech, American Portwell Technology, Intel Embedded Alliance

Next-generation Intel Atom processors deliver unprecedented power efficiency, graphics performance, responsiveness, and connectivity, enabling new products with groundbreaking intelligence and features. Examples include: Portable medical devices can last up to 10 hours on a single charge; low-cost network video recorders can incorporate sophisticated analysis software; rugged equipment can withstand extreme conditions thanks to lower heat dissipation. Learn what makes these Intel Atom processors a great fit for intelligent embedded systems and how you can get started quickly with boards and modules from the Intel Embedded Alliance.

Figure 3 | FMC board with four floating-point coprocessors for FPGAs

from BittWare, shown in Figure 3. Carrying a total of 64 cores on 4 coprocessors, it can be integrated on to any FMC carrier FPGA card, facilitating rapid deployment on both 3U and 6U VPX, convection or conduction cooled.

From the perspective of the FPGA, the coprocessor looks much like an embedded core. The coprocessor endpoint core sits directly on Altera's Avalon fabric. This tight integration gives it direct access to data inside the FPGA (and vice versa). The coprocessor software tools support fine-grained interaction with the FPGA, as well as direct host access and code debug through the FPGA. Of course, the coprocessor is much faster than any internal core and uses very little power.

FPGAs made perfect?

It has been well understood that the inherent flexibility of an FPGA does not come for free. Many attempts to mitigate these costs have been tried in the past, but none of these has proven effective or achieved even moderately wide adoption. Adding an external coprocessor to FPGAs is a new approach that promises to finally succeed in bring C to FPGAs. This offers system designers the best of both worlds: the flexibility and massive resources of FPGAs combined with the ease of use and power efficiency of a programmable multicore processor, thus eliminating the need for DSPs. This approach could prove ideal for embedded applications in the evolving modern-day military that increasingly require high performance, productivity, flexibility, and adaptability – all while improving SWaP. **MES**

Jeff Milrod, *realizing the futility of pursuing a career in music (and reluctantly admitting that his dad was right), went back to school and got a Bachelor's degree in Physics from the University of Maryland and later an MSEE degree from The Johns Hopkins University. After gaining extensive design experience at NASA and business experience at Booz, Allen, Hamilton, Jeff merged his technical expertise with his improvisational skills, starting Ixthos in 1991 – one of the first companies (along with BittWare) dedicated to COTS DSP. He ran Ixthos until it was acquired by DY4 Systems (now Curtiss-Wright Controls Defense Solutions or CWCDS) in 1997. Jeff left in 1998 and took the helm of BittWare, where he is President and CEO.*

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FPGA-powered display controllers enhance ISR video in real time

By Jason Wade and Randall Millar

The military relies on video imagery for situational awareness, but image quality is often so poor that operators can miss important details. Outfitting display controllers with FPGAs that run image enhancement algorithms in real time gives viewers a much better picture.

U.S. Air Force photo by Master Sgt. Daniel Richardson

The backbone of modern defense capabilities, Intelligence, Surveillance, and Reconnaissance (ISR) relies on a robust and diverse network of integrated sensors, aircraft, and manpower. The value of this network ultimately relies on human capability to clearly see sensor imagery, discern important details, and take decisive action. In the field, we have little or no control over the lighting and environmental conditions under which images are acquired from a sensor. It is possible, however, to give more control to the person viewing live sensor imagery, by allowing them to fine-tune video imagery on-the-fly to pull out more information.

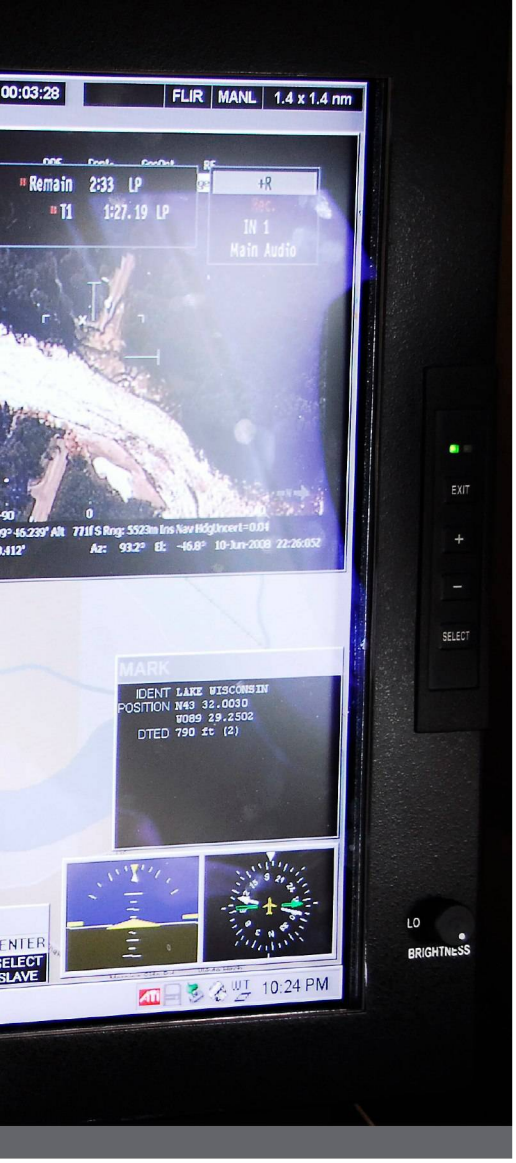
Enhancing video in real time requires tremendous computational throughput. It requires applying sophisticated image processing algorithms to incoming video streams without introducing delays. High-performance Field Programmable Gate Arrays (FPGAs) provide an ideal platform that allows software algorithms to be implemented using parallel computing techniques. When embedded into an intelligent display controller, these algorithms give operators maximum control over image quality, and result in dramatically better image clarity.

Clarity is in the eye of the beholder

Full-Motion Video (FMV) is the tool of choice for military situational awareness. Automated video recording is featured on virtually all military vehicles, including manned vessels such as fighter jets, trucks, and tanks, as well as Unmanned Aircraft Systems (UASs). Producing high-quality imagery on a mobile platform poses a number of challenges. In addition to issues related to camera motion and the resulting image perspectives, the quality of the video imagery can also be compromised by poor environmental conditions, data link degradations, and bandwidth limitations. Atmospheric factors such as poor lighting at dawn, dusk, or nighttime, and adverse weather, including sandstorms and variable clouds, can obscure important details.

Sensor image quality, however, is not the only problem. The conditions under which the video is viewed vary widely and thus present another set of challenges. For example, video streams may be viewed in bright sunlight, under water, or in a dark cave with a headlamp shining on the screen. Because of this, there is a distinct advantage in providing image enhancement capability within the display itself, rather than at the sensor or elsewhere on the network.

The only way to ensure a good image quality is to give the viewer the ability to adjust the picture for their needs. The best way to accomplish this is to bring real-time video enhancement to the tactical edge. FPGAs offer the performance,



design flexibility, and resilience needed to build this capability directly into the display controller.

A video controller with real-time image enhancement

All display controllers perform basic image processing, which means they take in video at a certain resolution and display it in the display's native resolution. For example, if it's a 1,920 x 1,080 display, it needs to receive 1,920 x 1,080 pixels for every frame. However, there is no guarantee that a user is going to plug in a raster that matches that; in fact, odds are he won't. Instead, the incoming video stream might be formatted 1,024 x 768 or similarly. Video processing is the act of scaling, which is converting an incoming video signal from one size or resolution to another in order to work with the display panel. This is what is usually referred to as "video processing," and it is a minor feat compared to video enhancement.

> "... Video streams may be viewed in bright sunlight, under water, or in a dark cave with a headlamp shining on the screen. Because of this, there is a distinct advantage in providing image enhancement capability within the display itself, rather than at the sensor or elsewhere on the network."

Video enhancement begins where video processing ends. A video controller designed for real-time video enhancement might start with an off-the-shelf video processing chip or a purpose-built ASIC that does the scaling and basic image processing up front. Once that operation is complete, the video stream would then be handed off to a special purpose processor such as an FPGA for enhancement.

There is, of course, the option of combining both the video processing and video enhancing functions in a single ASIC. In fact, that is what manufacturers of consumer television often do. However, this implementation is best suited for rudimentary video enhancement, such as edge sharpening, and leaves little room for sophisticated image enhancement algorithms. With an FPGA that is dedicated to real-time video enhancement built into the display controller, it is possible to reach beyond conventional display functionality and deliver advanced enhancement capabilities (Figure 1).

Amazing algorithms are computationally intensive

Anyone familiar with photo editing programs, such as Adobe Photoshop, can appreciate the power of software algorithms for enhancing still images. Using sophisticated software algorithms to apply mathematical functions to the image matrix, it is possible to reveal hidden layers of visual information without losing detail. This is a purely mathematical approach that utilizes all of the available image information, including portions that are not normally visible to the human eye.

Over the past decades, a large body of image processing algorithms has been developed using techniques including histogram manipulation, convolution, morphology, over- and undersampling, quantization, and spectral processing, including Fourier transforms and Discrete Cosine Transforms (DCTs). These algorithms tend to be computationally intensive. Conventional processor technology does not offer the performance necessary to keep

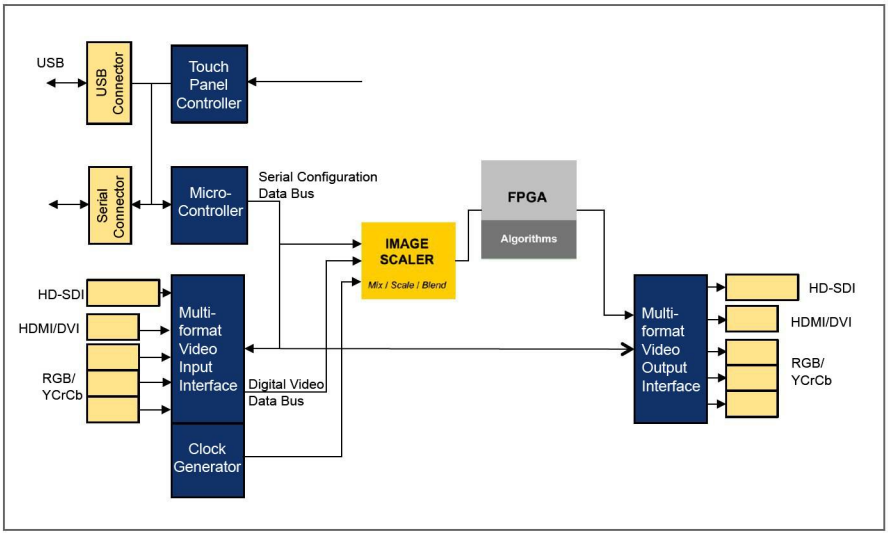


Figure 1 | Display controller with built-in, real-time video enhancement: A video processing chip formats the incoming video stream to match display requirements. The FPGA runs image enhancement algorithms to achieve dramatically better image clarity.

up with the demands of FMV at up to 60 frames per second (fps), or 1 frame every 16.67 milliseconds. Processing a Standard-Definition (SD) video stream requires about 150 to 200 Gigaflops, while a 1,080p stream requires about 1.2 Teraflops. This is where FPGAs come into play.

Convolution kernel filtering at work

When image enhancement algorithms are rewritten using parallel processing techniques and ported to an FPGA, it is possible to dramatically enhance ISR video in real time. Of the many types of image enhancement algorithms, spatial convolution kernel filtering produces the most dramatic results.

While the underlying mathematics of convolution filtering are complex, performing an image convolution operation is straightforward. A convolution kernel generates a new pixel value based on the relationship between the value of the pixel of interest, and the values of those that surround it. In convolution, two functions are overlaid and multiplied by one another. One of the functions is the video frame image and the other is a convolution kernel. The frame image is represented by a large array of numbers that are pixel values in x and y axes. The convolution kernel is a smaller array, or a mask where values are assigned based on the desired filtering function, for example, blur, sharpen, and edge detection. The size of this array, called the *kernel size*, determines how many neighboring pixels will be used to generate a new pixel. In convolution, the kernel operates on the image to create one new pixel each time the mask is applied, and therefore the operation must be repeated for every pixel in the image (Figure 2).

Large kernel yields better results

Convolutions are computationally intensive and therefore most implementations use only small kernels (3 x 3, 9 x 9, 16 x 16). However, using unique, non-traditional programming techniques, it is possible to implement very large convolution kernels that produce dramatically better results. The reason a very large kernel produces better results has to do with the range and variations in brightness over a given area, which is referred to as *spatial frequency*.

By considering the data in a large neighborhood centered around each pixel as it is being processed, a large kernel includes a much greater range of spatial frequencies. Traditional small kernel processing can only enhance details in the very highest spatial frequencies, which typically contain little of the spectral content (full range of color) of the image, and is where noise is prevalent. Hence, small kernel processors must employ high gain to have much noticeable effect on the image. High gain tends to produce sharp outlining artifacts and increases visible noise. Large kernel processing (operating on much more of the "meat" of the image) can produce dramatic results with much lower gain, with the additional benefits of large area shading, yielding much more natural-appearing images with increased local contrast, added dimensionality,

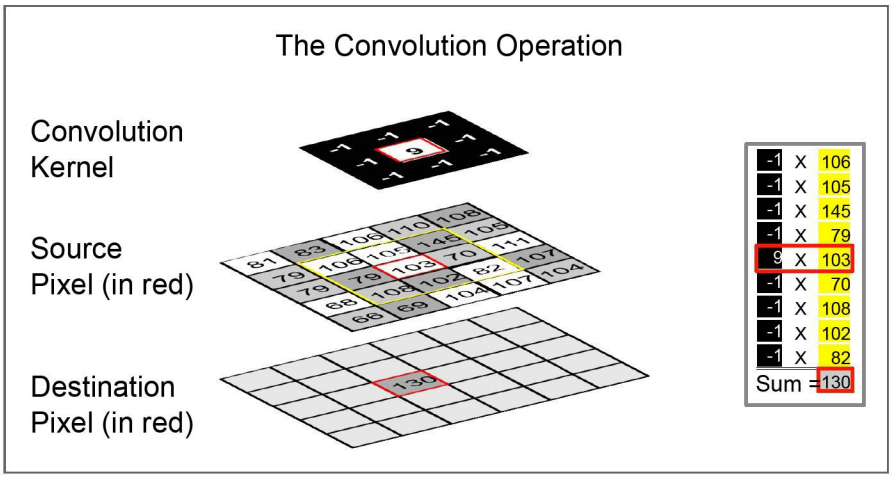


Figure 2 | Convolution kernel mask operation: The source pixel is replaced by a weighted average of itself and its neighboring pixels.

and improved visibility of subtle details and features.

One large kernel convolution algorithm, designed to clarify the image by removing haze and enhancing image detail, uses a 400 x 400 kernel. This clarifier algorithm works by solving a mathematical equation that relates a model of a "perfect image," to the measured imperfect image captured by the sensor camera. The technology works backwards, stripping corrupting noise and image blur while simultaneously adjusting the intensity of each pixel until the simplest image that fits the real-time data emerges.

The concept is that because it is known that environmental factors distort the image, if it is known how the distortion is created, then it can be undone. Other technologies use methods that strip out distortions and get close to the true image, but stop there. In contrast, this method takes a step further by continuing to apply the algorithm to the image until it is as close to the perfect image as possible. Thus, it is able to strip out all unnecessary data that is not part of the true image. Remarkable clarity is achieved once the environmental distortions are removed and as more of the real image reveals itself (Figure 3).

Figure 3 | Algorithms reveal unexpected detail: Picture-in-Picture shows the remarkable clarity achieved once the environmental distortions are removed.

Striving for a perfect image

FPGAs unlock the door to a vast array of sophisticated algorithms that can be used to enhance ISR video in real time. FPGAs are computational workhorses and well suited to military video display controller applications. They can withstand harsh environments and meet exacting military requirements for ruggedness, temperature tolerances, reliability, and a guaranteed long product lifespan. Because they are reprogrammable, FPGAs enable design flexibility so that a display controller can be readily adapted to changing video standards, or special mission requirements. Furthermore, once deployed, FPGA-based display controllers can be field upgraded to add additional features and new image enhancement algorithms. **MES**

Jason Wade *is the Vice President of Product Marketing and Sales at Z Microsystems. Previously, he was the company's Director of Engineering. Jason regularly works with the USAF and UAS suppliers to help solve technical problems that enhance UAS performance. Jason earned Bachelor of Science degrees in Applied Mathematics and Physics from UCLA and an MBA in Technology Management from UC Davis. Jason can be contacted at jason.wade@zmicro.com.*

Randall Millar *is Vice President of Engineering at Z Microsystems and oversees all facets of product development from conceptual design through delivery to the customer. "Randy" has extensive technical experience in the design of video processing systems and has been granted a number of patents for his work on real-time enhancement algorithms for the medical, military, and consumer markets. He earned his degree in Electrical Engineering at UCSD. He can be contacted at randall.millar@zmicro.com.*

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From Wall Street to the military:

Advances in FPGA switching technology and software-to-hardware development tools facilitate wire-speed data transmission

By Douglas Gourlay and Brian Durwood

Reversing the historical trend of the U.S. military being the first to develop key technologies that fan out to the rest of society – such as the Internet, radar, and lasers – Wall Street is now funding ultra-low-latency data transmission technologies facilitated by advanced FPGA switching techniques and unconventional software-to-hardware development tools.

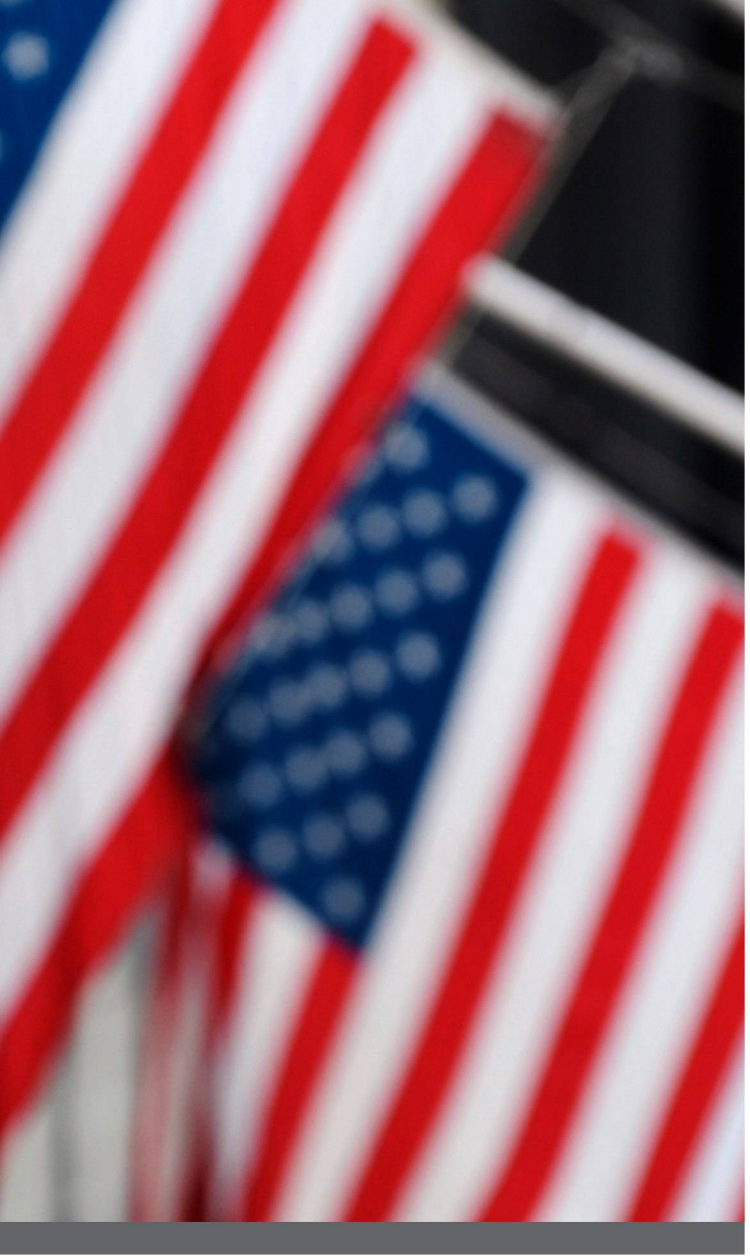
For federal agencies, the military, and other segments of modern society, there is an increasing world of data that would ideally be processed at full resolution and at wire speed. *Wire speed* means full data rate and as close to zero latency as possible such that there is no lag, no buffer, and no writing to memory. *Full resolution* means that there has been no compromise on the data stream sampling. This is significant, as some systems achieve wire speed only by reducing the sampling rate.

Meanwhile, the backbone of the Internet today is increasingly Ethernet network switches and routers. Recently there have been generational advancements in switch technology, where a programmable processing element is added very close to the ports and on the same mainboard as the rest of the switch hardware. The processing element is an FPGA, which comes off the shelf with more than 5 million logic elements. FPGAs are best suited to this location because of their parallel processing capability and higher, more flexible input and output options as compared to an ASIC. This provides the ability to instantiate a semicustom multicore computer at the edge of the wire. FPGAs in this use are ultra-low latency, programmable, and very flexible; however, software developers must learn a few new tricks to efficiently move their C algorithms to an FPGA.

Technology "trickle up"?

In an odd reversal of historical U.S. military "trickle down" by which government technology investments brought industry the Internet, radar, and the laser, development of this ultra-fast FPGA switch technology is being funded by Wall Street where winners and losers are separated by nanoseconds. What Wall Street discovered was that acceleration by parallelism trumps acceleration by clock speed. So as microprocessors approach limits of single-core clock speeds, efforts are shifting to "multi-core" and extending parallelism. Basically for nonsequential logic, each process that can be run in parallel increases system throughput fairly linearly. Throughput often doubles with the first few parallelizations.

The latency and throughput effort shifting towards parallelism has FPGAs coming into prominence as processors in military technologies and elsewhere. Even at FPGAs' slower clock speeds (and cooler operation), their extreme advantage in I/O and the ability to provide multiple cores enable FPGAs to



be deployed at lower latency than traditional microprocessor implementations. FPGAs have been clocked at 2 microseconds in round-trip, wire-to-wire transactions. The optional soft-core processors allow code to be partitioned, some to compile into FPGA hardware and some to run "natively" in the onboard processor core (Figure 1). Or multiple parallel processes can run "natively" on multiple cores in the programmable switch.

The trend

To create seamless network insertion with a programmable dataplane represents an advance. The legacy option to use an appliance and somehow glue it to a switch or router has evolved into a fully capable switching and routing node that handles access control, QoS, and forwarding logic coupled with an inline programmable subsystem that is directly integrated with the forwarding plane, resulting in 24 1/10GbE wirespeed ports in a compact 1RU chassis. The integrated subsystem is optimal to run latency-sensitive and mission-critical applications directly in the switch, improving performance and determinism while reducing overall latency and costs. A built-in SSD is included for advanced logging, data captures, and supporting embedded applications. The application switch subsystem includes an Altera Stratix V FPGA with 160 Gbps of wire-speed performance and 6.2 million gates.

How to work with this technology

Programming many gates in a hardware description language is time consuming and increasingly an uncommon skill. This has instigated a shift toward compiling software to hardware. This shift has software teams scrambling to understand the differences. Tell a software developer that memory is no longer free and that access to I/O requires hardware drivers, and their eyes glaze over. Explain how the final compile to hardware can take hours and they begin to worry. Even with that, estimates are that there have been about 5,000 successful software-to-hardware projects completed in the past decade. The key is to stay as much as possible in a common High Level Language (HLL) such as C and to use tools to optimize the algorithm for operation on FPGA hardware.

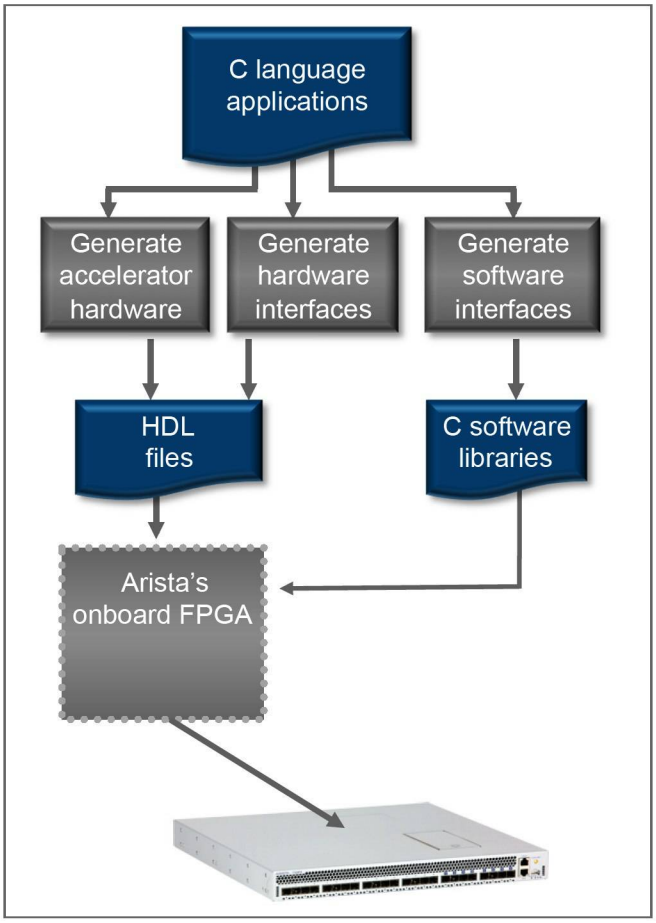


Figure 1 | C language files are partitioned to run in switch-integrated FPGA hardware or "natively" in C on the optional soft-core processor in the programmable switch.

Popular high-performance uses of this methodology include:

a. Inserting analytic modules or filters in-line: This is useful for algorithms for monitoring agencies like filters for unstructured data, FFTs, pass/no pass filters, and intrusion detection – anything that needs to operate at wire speed.
b. In security, inserting encryptors/decryptors with some type of activity flag is a common use as is wire-speed intrusion detection and lawful intercept.
c. On Wall Street, it's mostly data-based routing – stock symbols, SMS message content, compliance, and automated trading. The federal agency equivalent could be looking for specific data with zero or low latency (that is, at wire speed).
d. DSP functions such as signals intelligence and radar systems targeting technologies are also common.
e. Useful in deep buffers for long "fat" network satellite problems.

Typically design begins "device independent," where a C file is wrapped and brought into the tool flow. Analytics provide instrumentation to illustrate where there are opportunities for increasing parallelism or for how the stage delay propagates from specific lines of C. In the case of deep packet inspection, the focus of this design phase is typically the filters, wherein the designer iteratively refactors C to maximize parallelism (Figure 2).

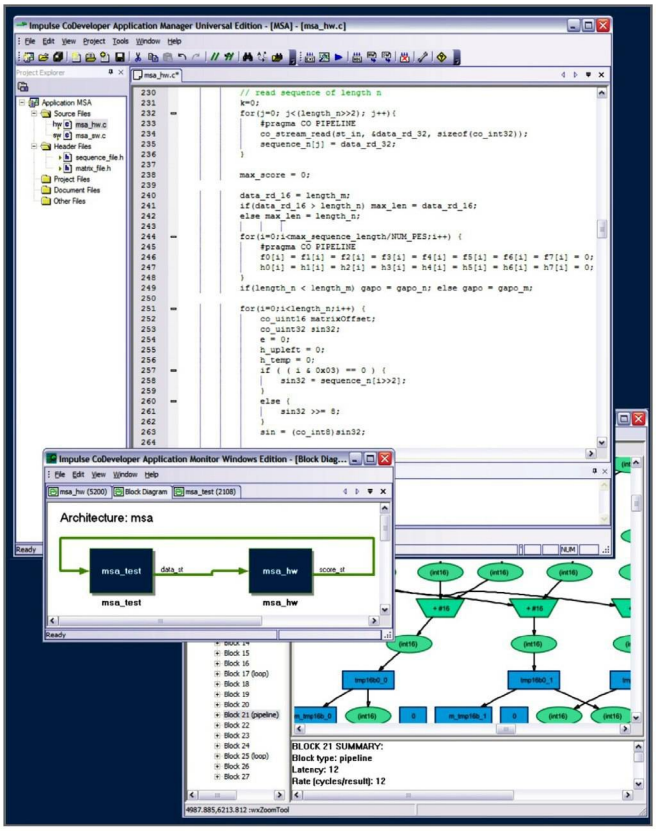


Figure 2 | The design flow starts with standard software development tools, analyzes flow for blockages, then provides detailed stage delay depiction and analysis.

Developers begin with untimed C, validating that the algorithm to run in hardware is equivalent to the original microprocessor-oriented version. The process from there is iteratively unrolling loops, increasing parallelism and reducing clock cycles. The Impulse C software-to-hardware compiler accepts untimed C. "Untimed" refers to C code that does not include additional information related to register boundaries, clocks, and reset logic. Impulse C automatically parallelizes C code, and there is no need to express such parallelism at the level of individual statements or blocks of code. To do this, it analyzes C code, finds interdependencies, and collapses multiple C statements into single instruction stages representing a single clock cycle. This automated creation of parallel hardware can be controlled by the programmer (for size/speed trade-offs) using compiler pragmas (Figure 3).

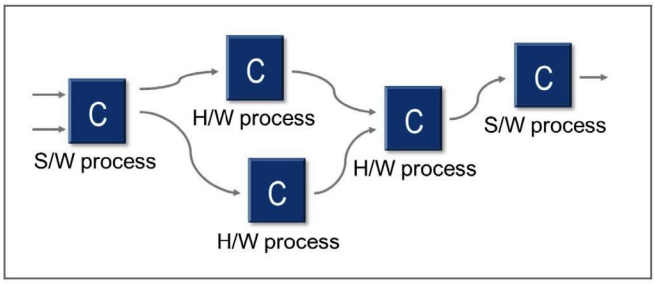


Figure 3 | Parallelism involves unrolling a software process into multiple parallel hardware processes.

Some of the early C-to-FPGA tools relied on PAR and other embedded hardware specific statements, which limited their ANSI C compatibility. Newer, more flexible tools defer the hardware-specific elements to as late in the design flow as possible to retain full ANSI C compatibility. First-level verification is done within Visual Studio or the equivalent. The output is synthesizable VHDL (or Verilog) with three uses:

1. It exports to the FPGA maker's place-and-route tool for compilation to gates.
2. It exports (optionally) to powerful simulators such as Mentor's ModelSim or Aldec's Active-HDL for cycle accurate simulation. Remember, the design involves more than 5 million gates, so verification at each step is critical.
3. Some key VHDL routines are segregated at this stage for hand optimization. The trick is to keep as much as possible in C, facilitating migration to next year's FPGA, and only hand-tweak the modules with the highest performance potential.

Hardware dependencies are inserted in a layer called a *Platform Support Package* (PSP). Here, board manufacturers create links to the hardware functions that can be accessed by C-level commands. This is sometimes referred to as the "plumbing." PSPs are typically provided as source for the development teams that need to modify them.

Acquiring known-good code is also increasingly common in rapidly deploying image processing, packet inspection, and

other processing-heavy tasks. Sometimes the code modules are for drivers and other noncritical elements, but increasingly highly optimized portions such as TCP/IP offload engines and encryptors can be acquired as Intellectual Property (IP). Acquiring known-good code cuts development time and improves performance. All of it remains ANSI C compatible, and even the new software-to-hardware functions make common sense to most software developers (Figure 4).

co_stream_create	Used in configuration
co_stream_open	Open the stream (clear eos)
co_stream_close	Close the stream (set eos)
co_stream_eos	Check end of stream (eos)
co_stream_read	Read from stream (with rdy, en)
co_stream_write	Write to stream (with rdy, en)
co_stream_read_nb	Non-blocking read (no rdy)
co_stream_write_nb	Non-blocking write (no rdy)

Figure 4 | Language elements familiar to C coders are added in to accommodate hardware yet maintain ANSI C compatibility.

New architecture = new opportunities for speed

Putting the FPGA into a programmable switch, as close to the wire as possible, creates a new trend in integrated platforms, which is rapidly gaining the interest of both Wall Street and federal agencies and soon the military. Working with the platform is a little different from classic microprocessor-based development, but still accessible to both hardware and software engineers. **MES**

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